# Materials and Devices beyond CMOS Transistor for Energy Efficient Computing

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Exploratory IC, Components Research

Intel

# Outline

- Moore’s Law scaling and the energy crisis
- Beyond-CMOS devices for lower energy
- Spintronics materials and devices
- Ferroelectric and multiferroic materials and devices
- Benchmarking of beyond-CMOS devices

# Moore’s Law

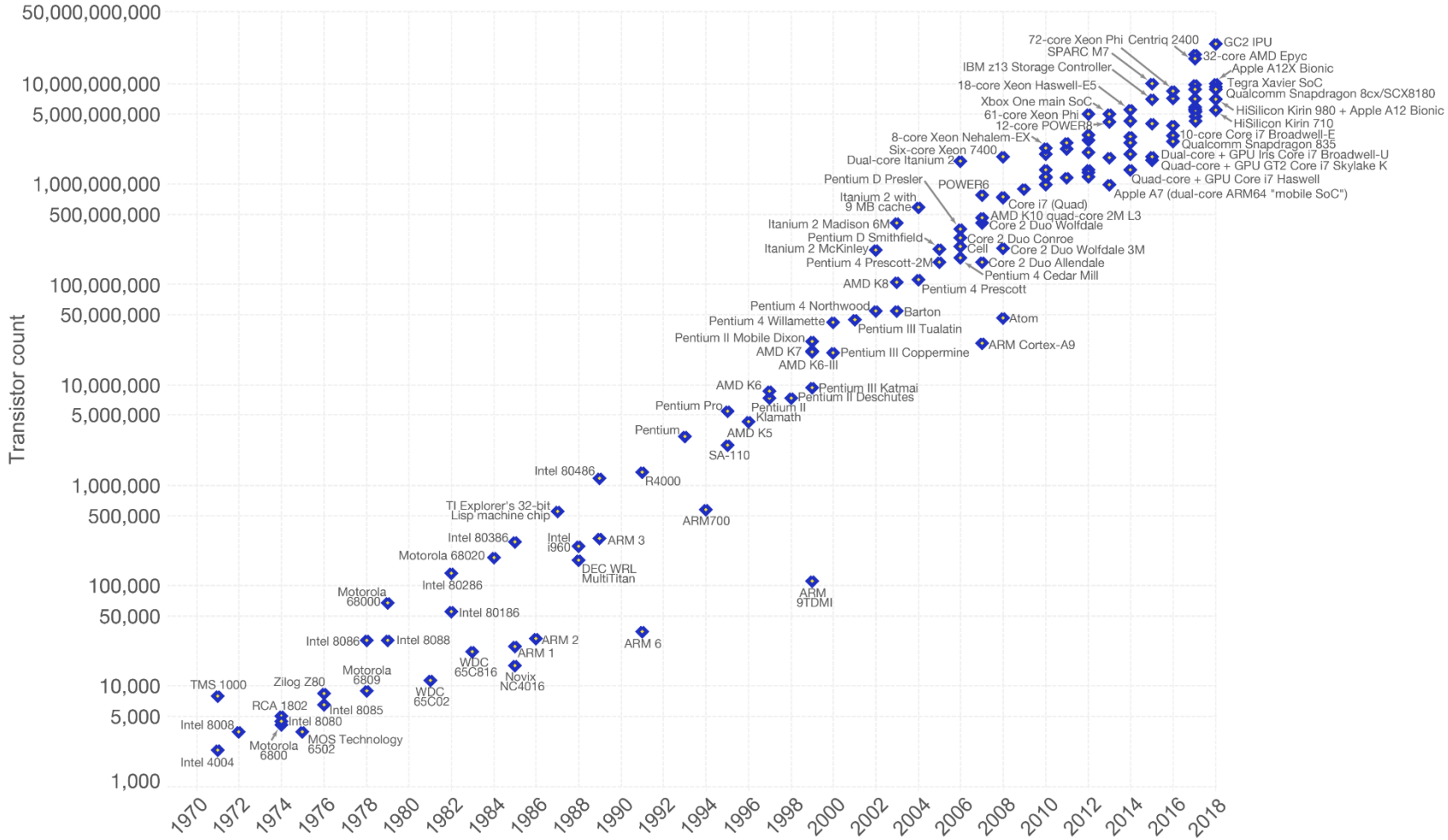
**Double the number of transistors on a chip every 2 years.**

Moore’s Law is Alive and Well

## Moore’s Law – The number of transistors on integrated circuit chips (1971-2018)

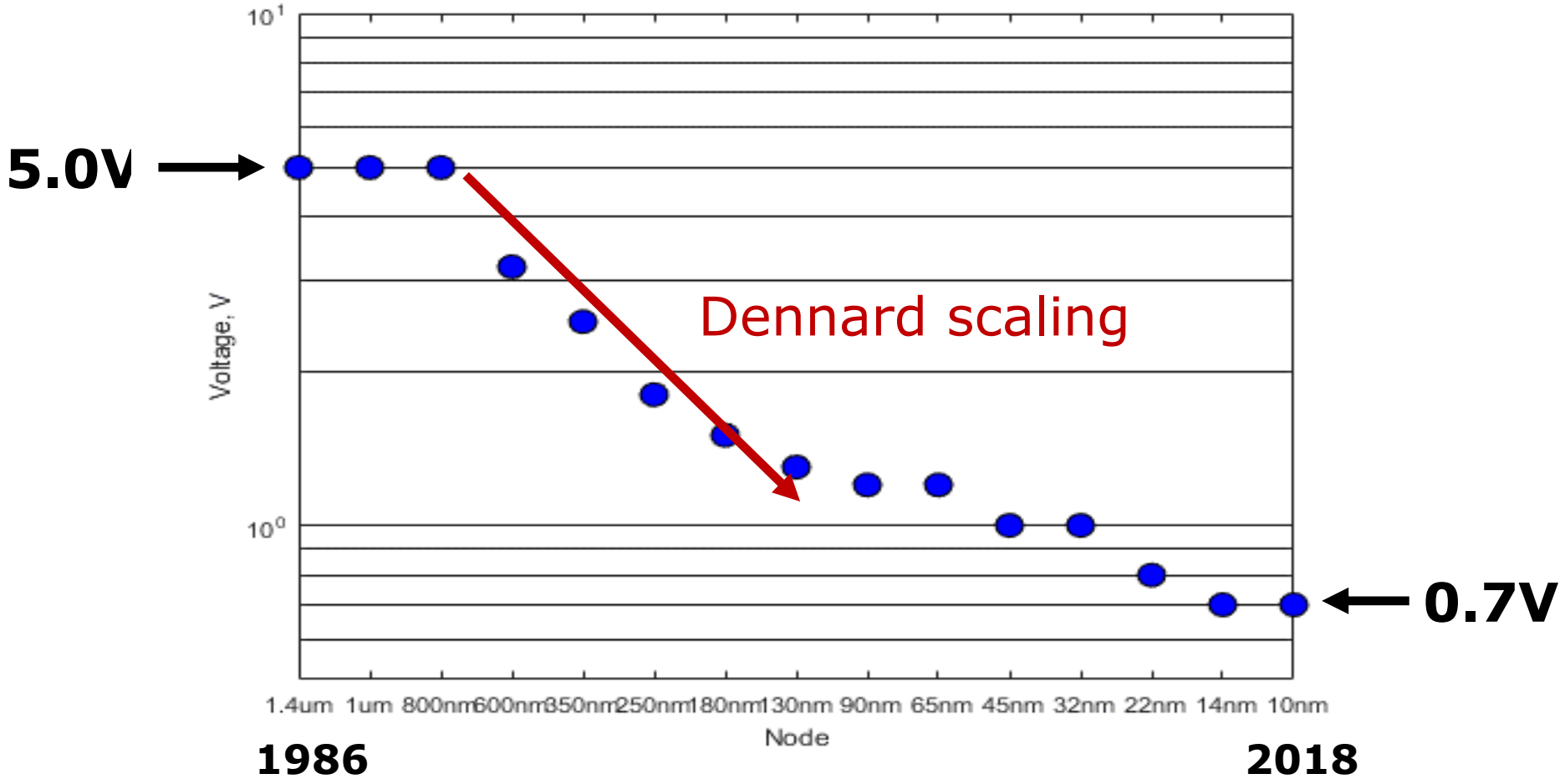
Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.

Our World in Data



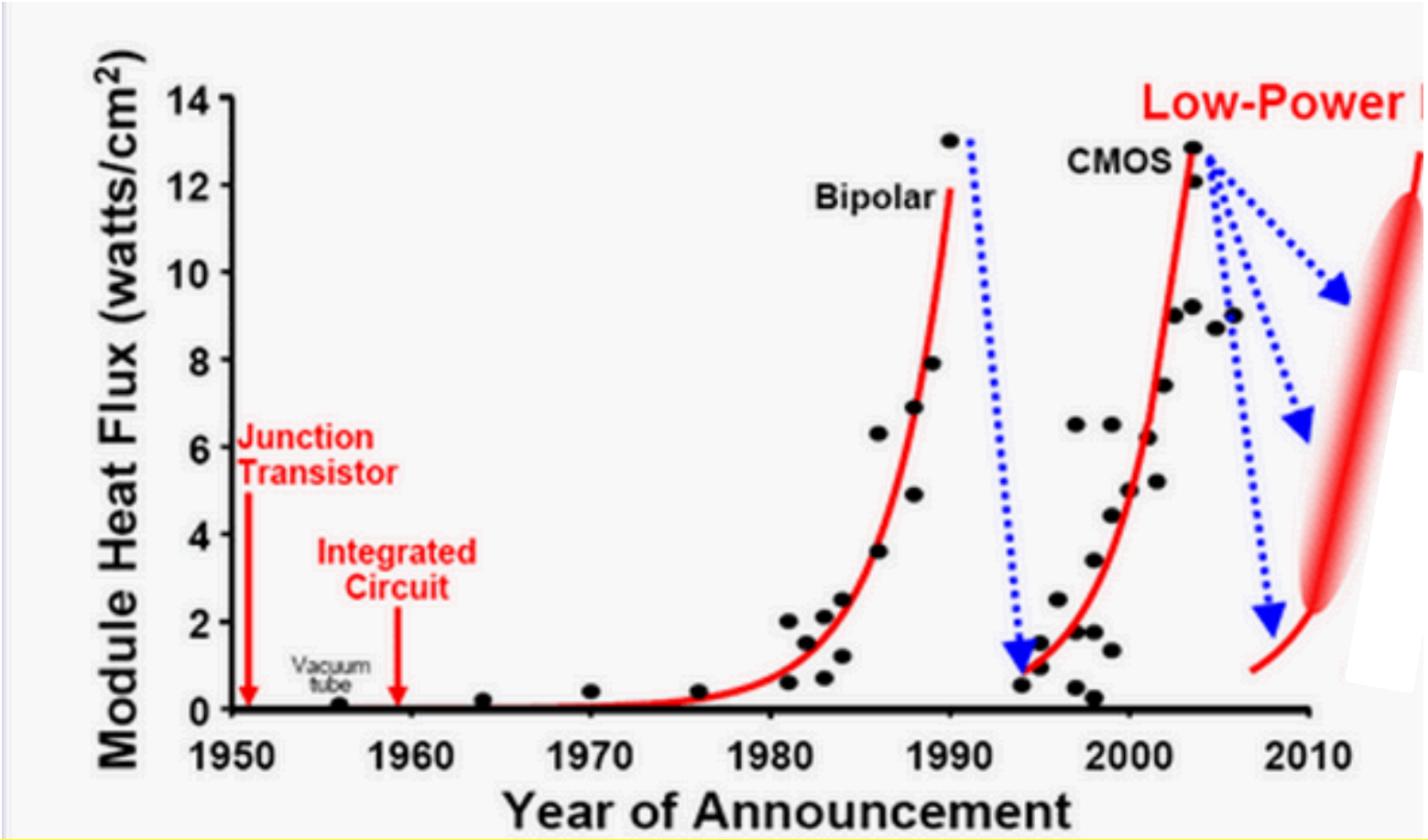

Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

# CMOS Supply Voltage - Historical Trend




In the last 15 years voltage scaling is stalled

# CMOS Challenge With Energy

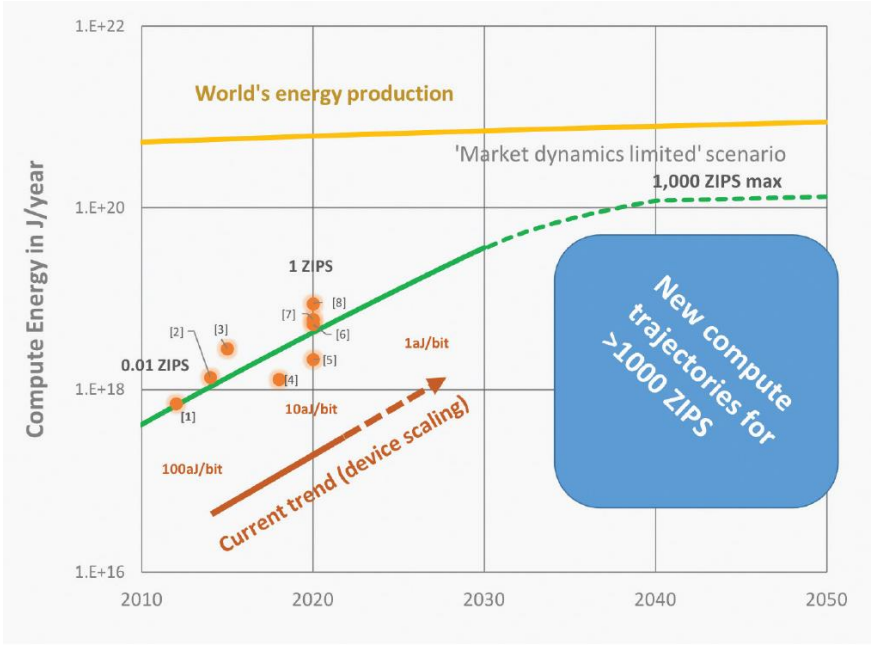


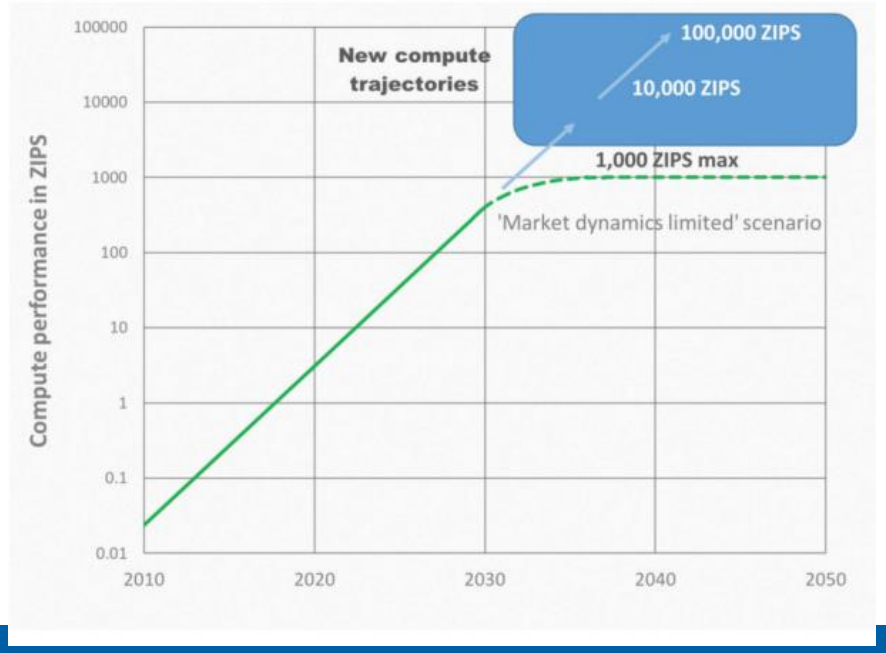

Semiconductor industry faced the power crisis before with bipolar transistors

*Source: Chen (IBM), ISS Europe, 2007.*

# Energy Crisis

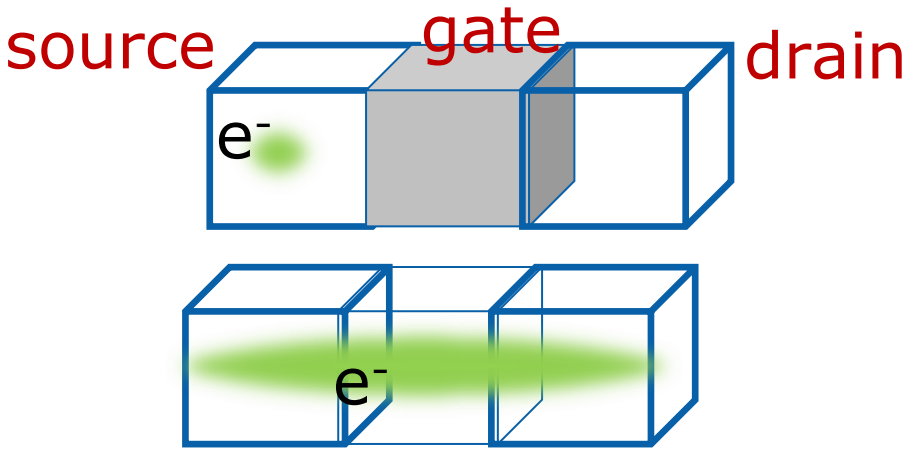
- Exploding demand for computing due to datacenters, AI
- Required energy will approach a few % of world production by 2030
- CMOS business as usual will lead to stalling IT, deficit of computing
- Need more energy efficient devices to continue sustainable development, curb carbon emissions

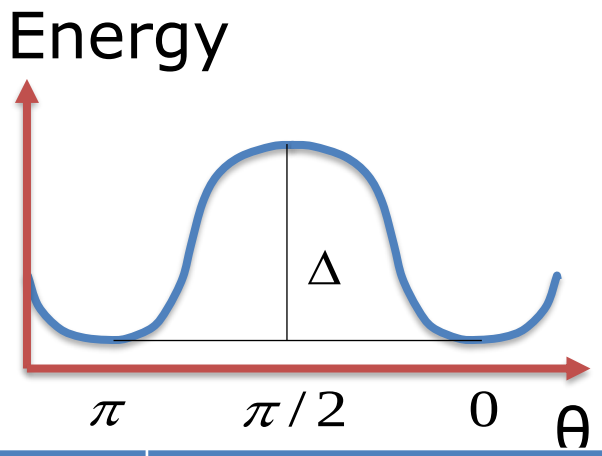



SRC, Decadal Plan for Semiconductors, 2021

# Collective States = Energy Efficiency




| | Generic Electronic Switch | Generic Spintronic Switch |
|---|---|---|
| Barrier | 20 kT (from Ion/Ioff) | 60 kT (non-volatile) |
| Voltage | 0.5 – 1 V | 10-100 mV |
| Particles | Ne = 200 electrons | Ns = 10000 spins |
| Sw. Energy Limit | 4000kT = Ne*20kT | 60 kT |
| Phenomenon | Non collective | Collective |

$$E = e\Delta VN \sim 4000kT \quad (1)$$

Leakage determined by barrier

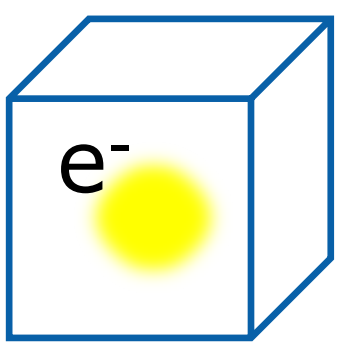
$$I_{on}/I_{off} < \exp(\frac{e\Delta V}{kT}) \quad (3)$$

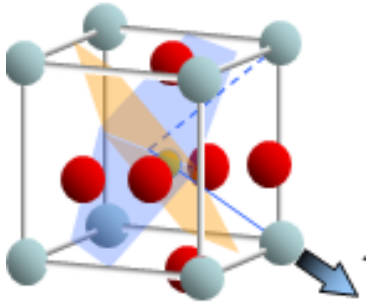
$$E = \frac{1}{2}\mu_0\mu_B N_s H_k \sim 60kT \quad (2)$$

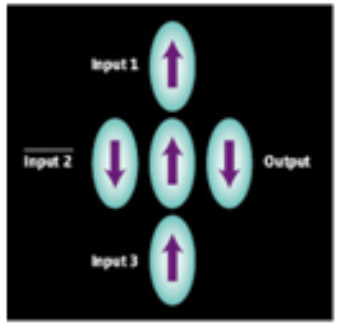
Leakage not related to barrier

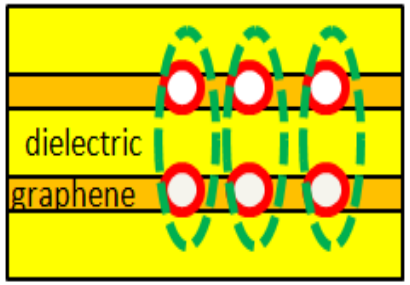
# 2 Collective States = Non-Volatility

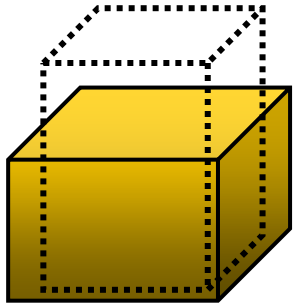
| Class | Variables | Example |
|---|---|---|
| Charge | Q, I, V | CMOS, TFET |
| Electric Dipole | P | FeFET |
| Magnetic Dipole | M, $I_{spin}$ | ASL, SWD, NML |
| Orbital State | Orb, Bose condensate | BisFET |
| Strain | $\sigma$ | PiezoFET |





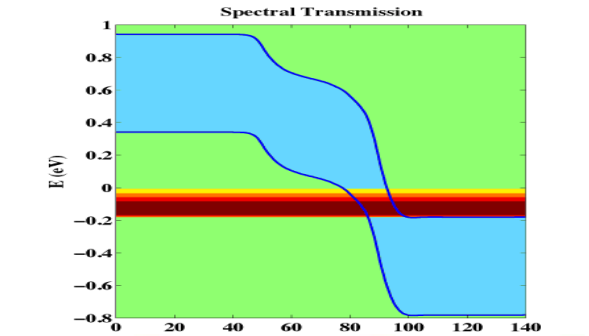
Charge | Electric Dipole | Magnetic Dipole | Orbital State | Strain

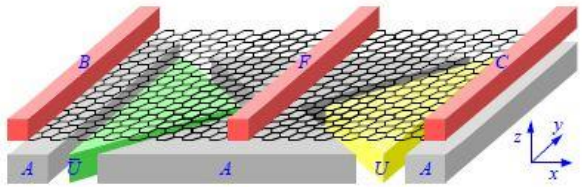
Can have non-volatile states at room temperature

# Beyond-CMOS Devices, part 1

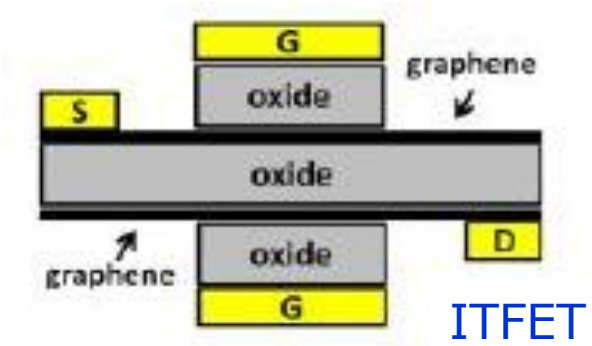
## Electronic

Tunneling FET- multiple!!!



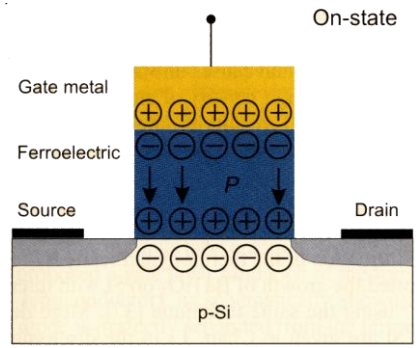




Graphene pn Junction



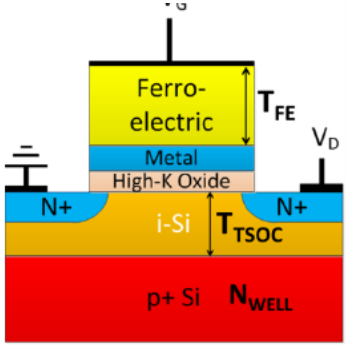

ITFET

## Ferroelectric

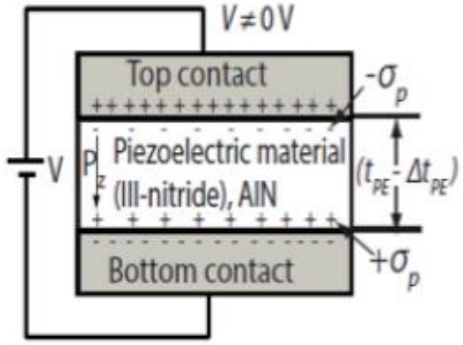



FEFET

Negative Cap FET

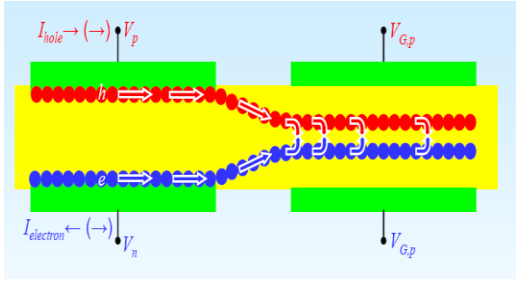



## Straintronic



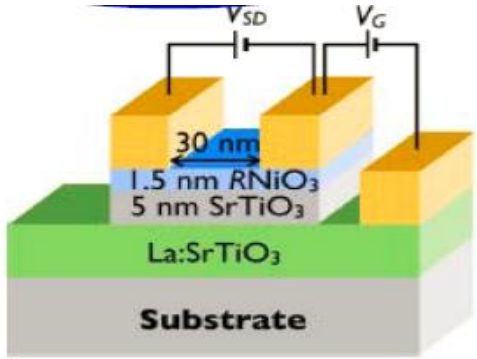

PiezoFET

## Orbitronic



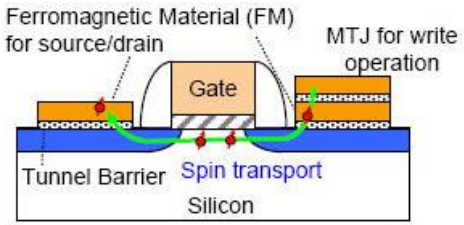

BisFET

MITFET

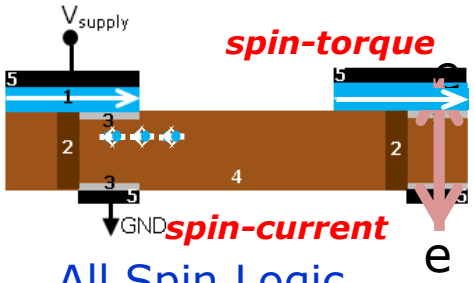


# Beyond-CMOS Devices, part 2

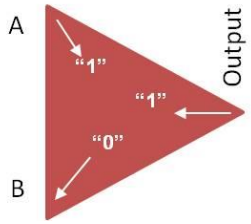
Spintronic



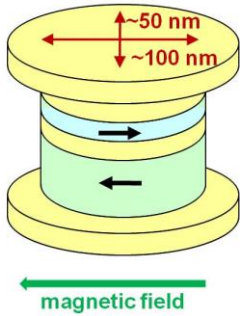

SpinFET



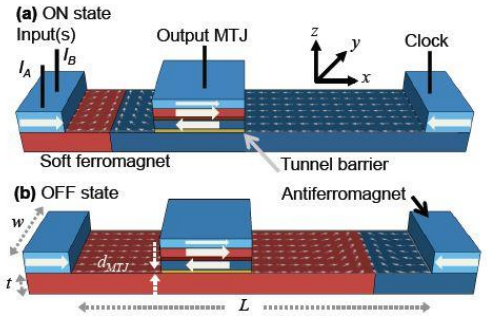

All Spin Logic



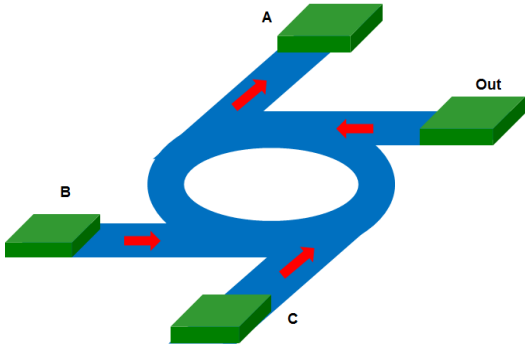

Spin Torque Triad



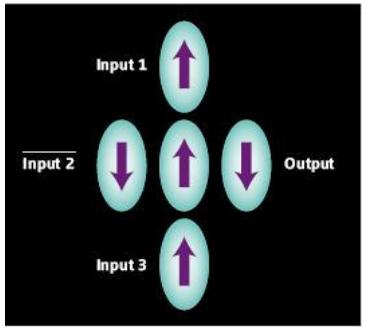

Spin Torque Oscillator



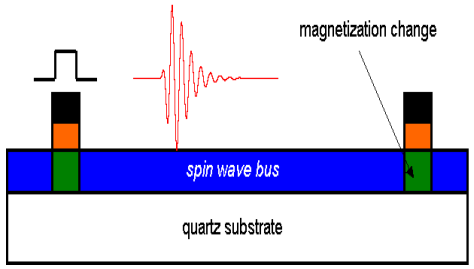

Domain Wall Logic



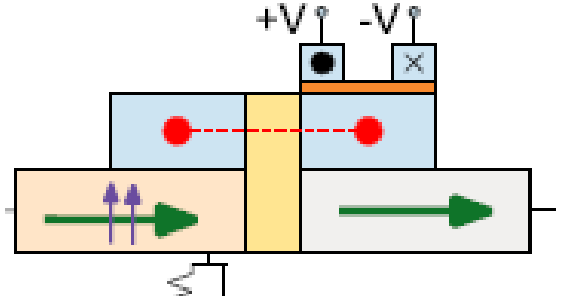

Spin Majority Gate




Nano Magnet Logic

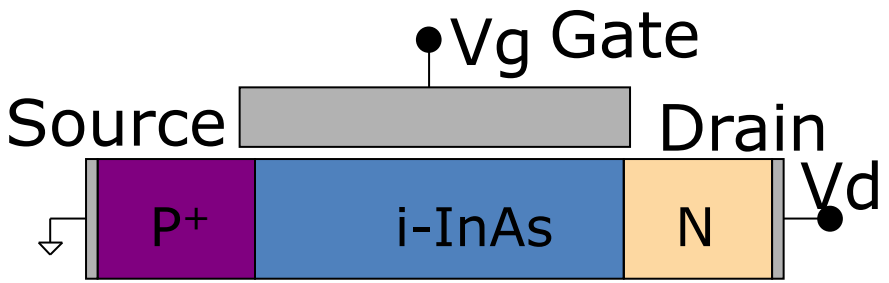


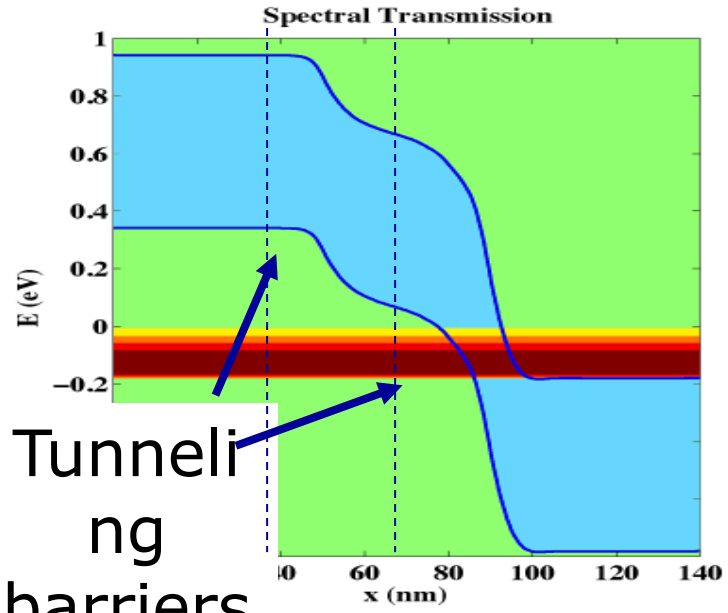

Spin Wave Device




Charge-spin logic

# Tunneling Field-Effect Transistor




Courtesy M. Luisier (Purdue)
M. Luisier and G. Klimeck, EDL, 2009

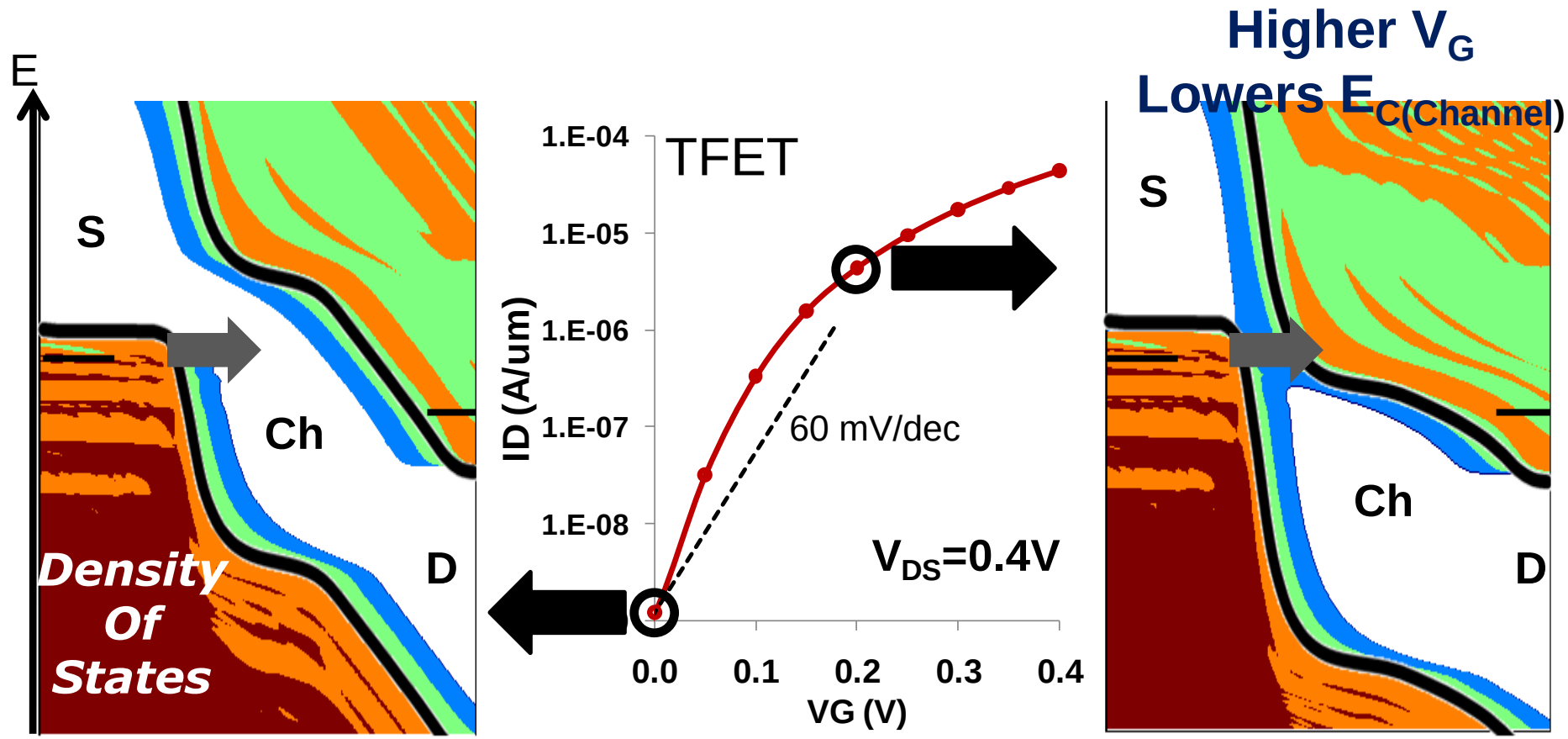
Tunnel FETs operate by tunneling through the S/D barrier rather than diffusion over the barrier

Two required conditions:

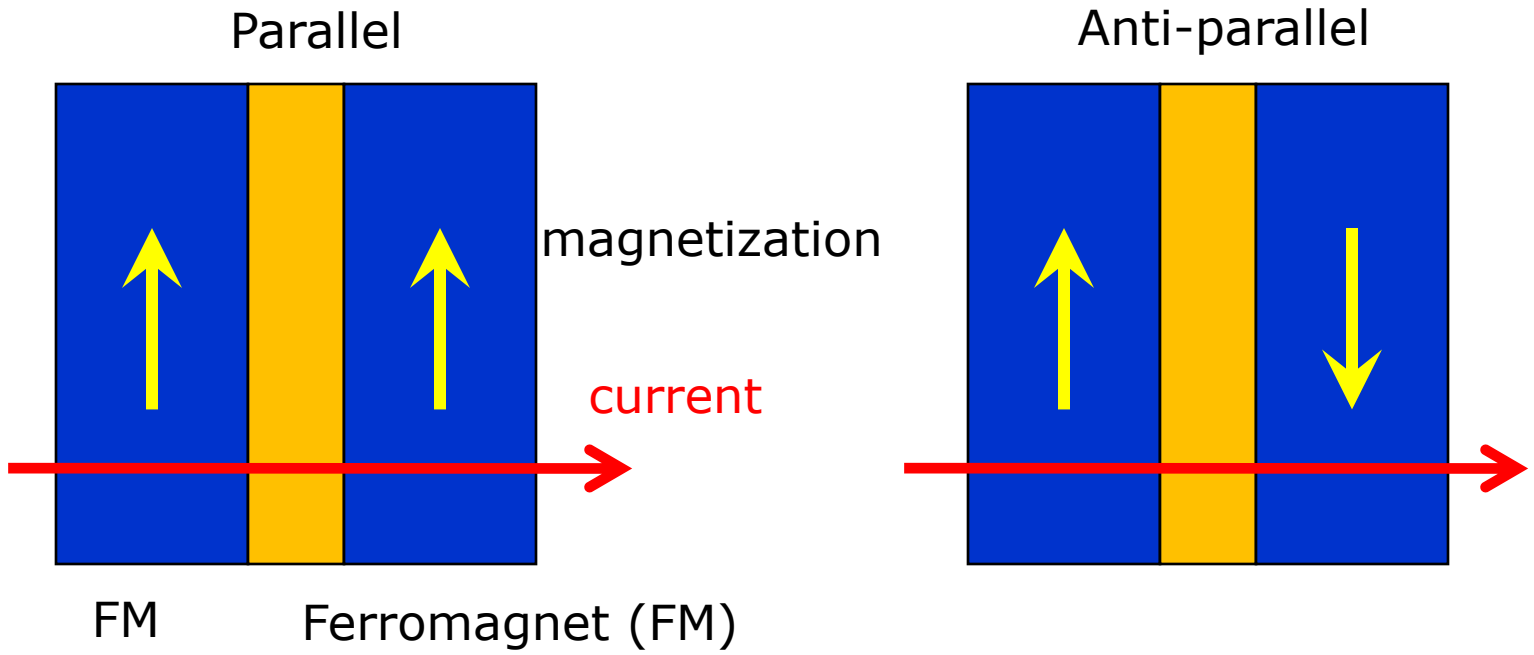
- Thin enough barrier over a large enough area for effective (high current) tunneling.
- Sufficient density of states on both the transmission and receiving sides to provide energetic locations for the carriers.

# TFET Sub-threshold Slope

Tunneling probability increases sharply at the onset of Source Valance Band and Channel Conduction Band overlap



# Magnetoresistance



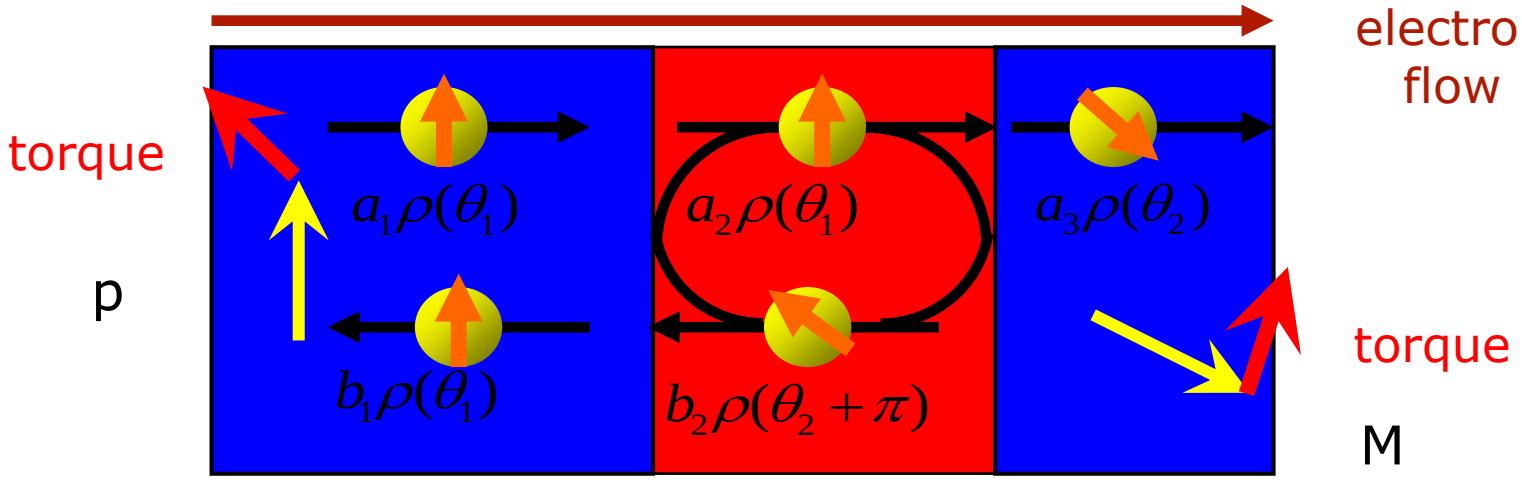

$$R_{AP} > R_P$$

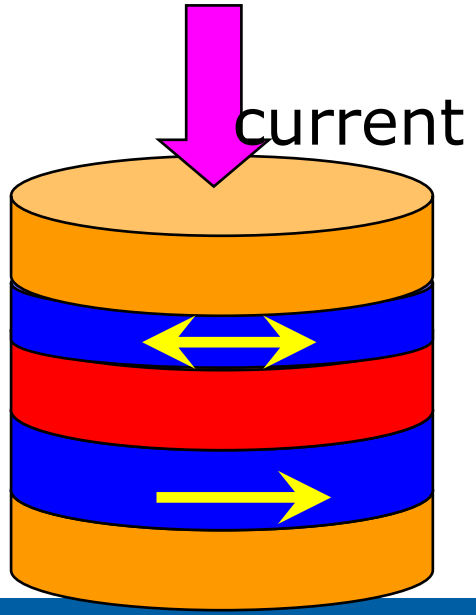
Resistance of the stack with anti-parallel magnetizations is higher

$$MR = \frac{R_{AP} - R_P}{R_P}$$

Magnetoresistance definition

# Spin transfer torque



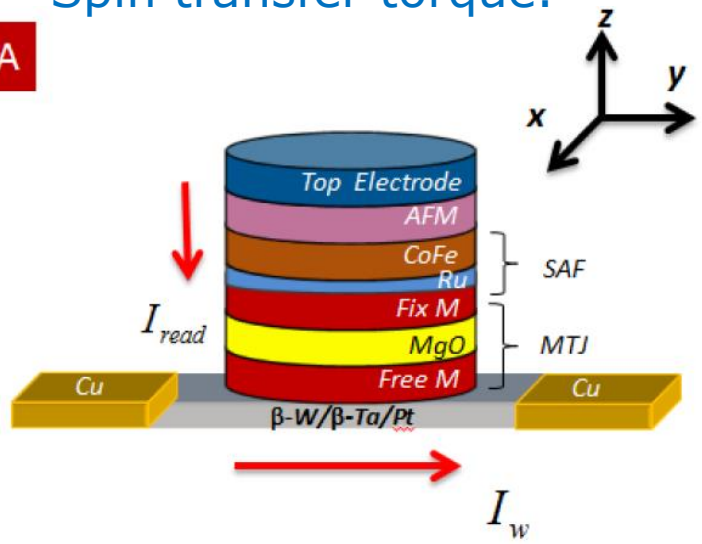

M = magnetization of free layer
p = polarization of injected electrons from pinned layer

Electrons get transmitted and reflected at the barrier
Each brings a unit of spin ħ/2
Combined transfer of angular momentum is torque, which rotates magnetization

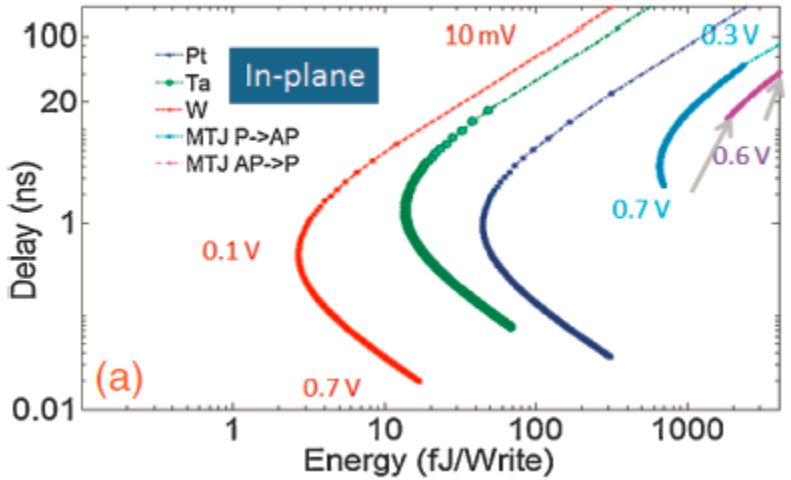
# Spin-Orbit Torque for Low-Power

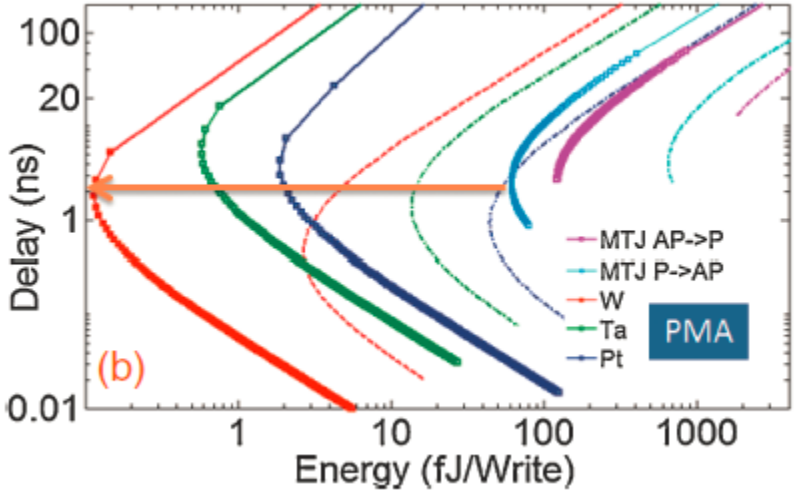
- **Need:** Operate memory and logic at 0.1V supply.
- **Method:** Macrospin switching by spin-orbit effect + spin drift-diffusion.
- **Result:** Spin-orbit effect produces faster magnetization switching at much lower voltage and energy than Spin transfer torque.

A

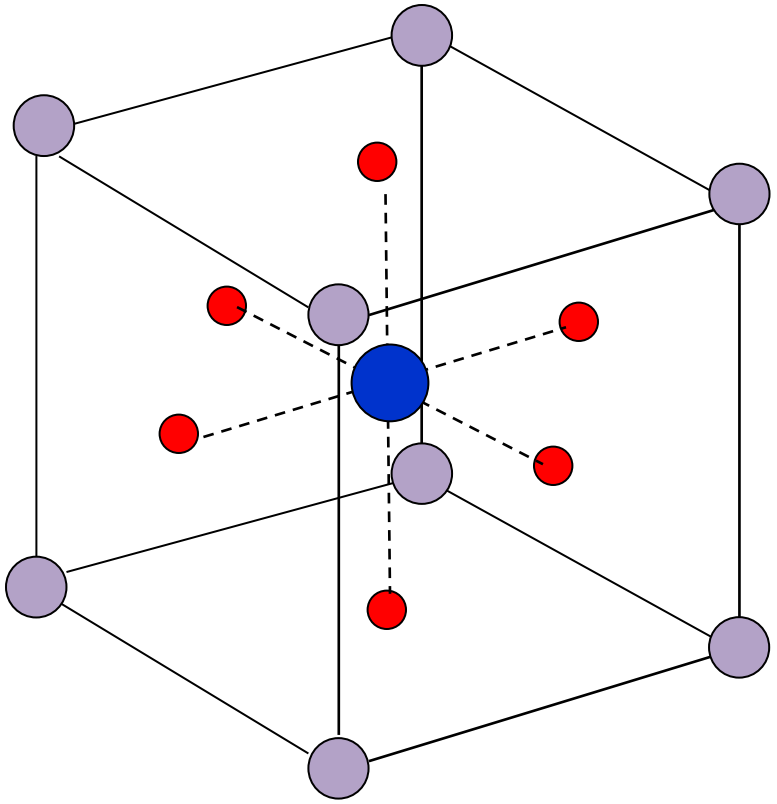


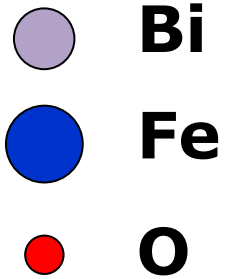

*S. Manipatruni, D. E. Nikonov, and I. A. Young, Appl. Phys. Exp. 7, 103001 (2014).*

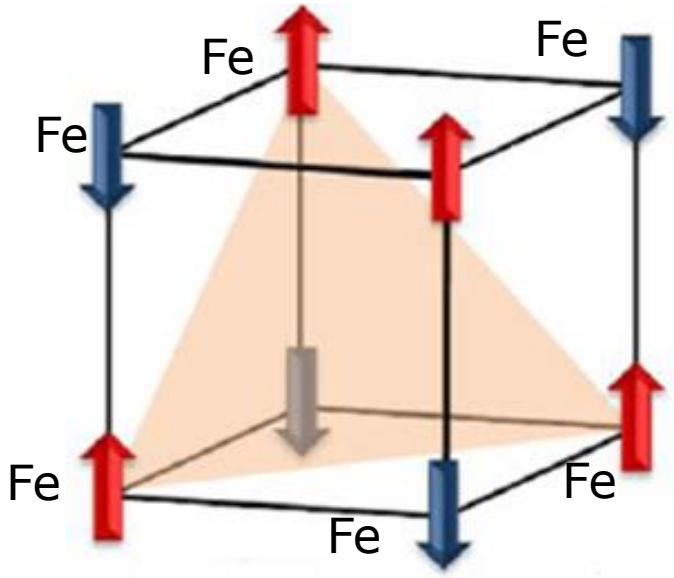


# Multiferroic BiFeO3





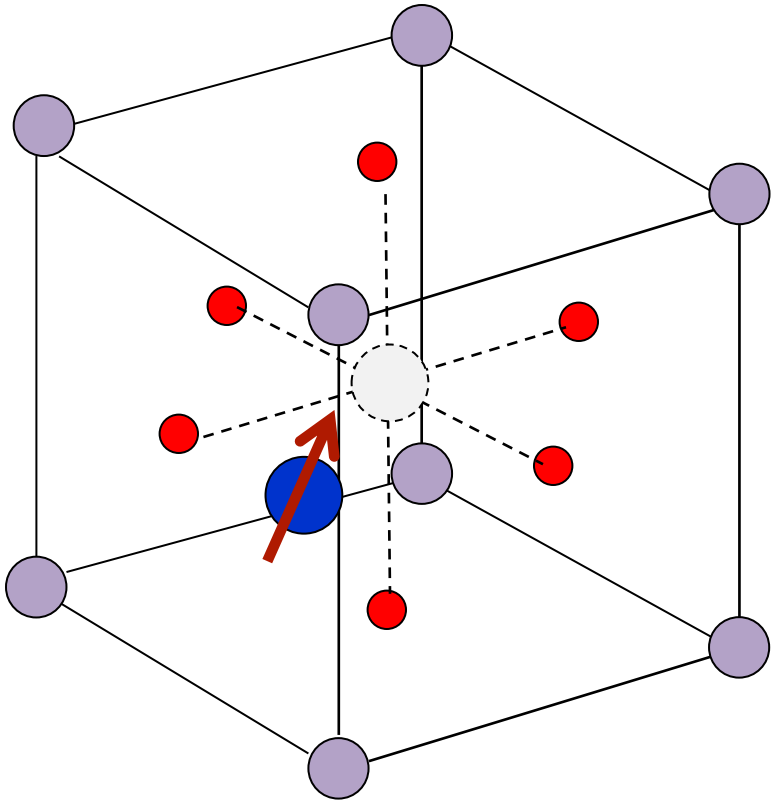



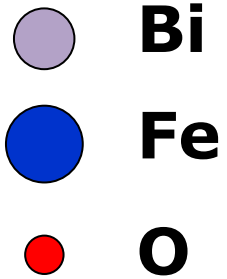

$BiFeO_3$

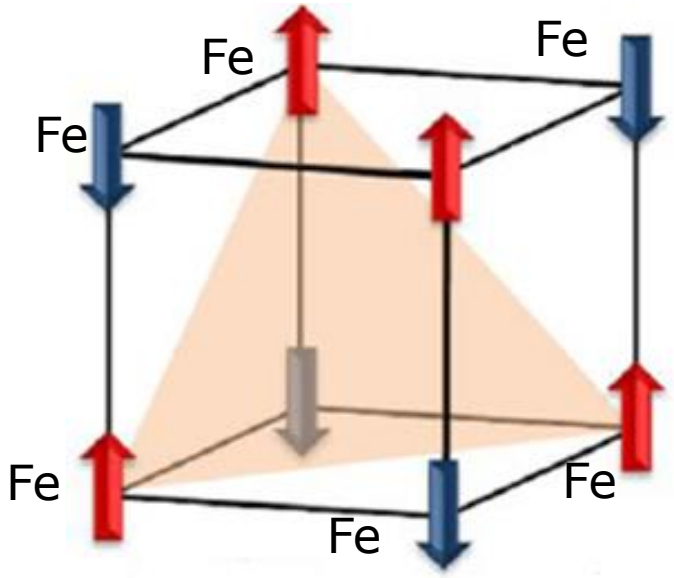
- Ferroelectric (FE) below $T_C$ = 1100 K
- Fe atoms shift to corner of the cube in E-field
- Antiferromagnetic (AFM) below $T_N$ = 640 K
- Spins on Fe interchange in direction
- So far one of 3 room temperature multiferroics

Coupling of electric and magnetic above room temperature

# Multiferroic BiFeO3



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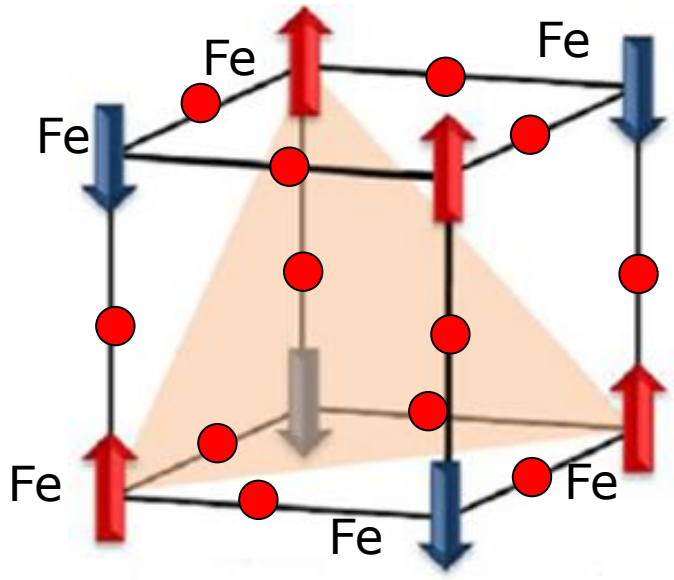
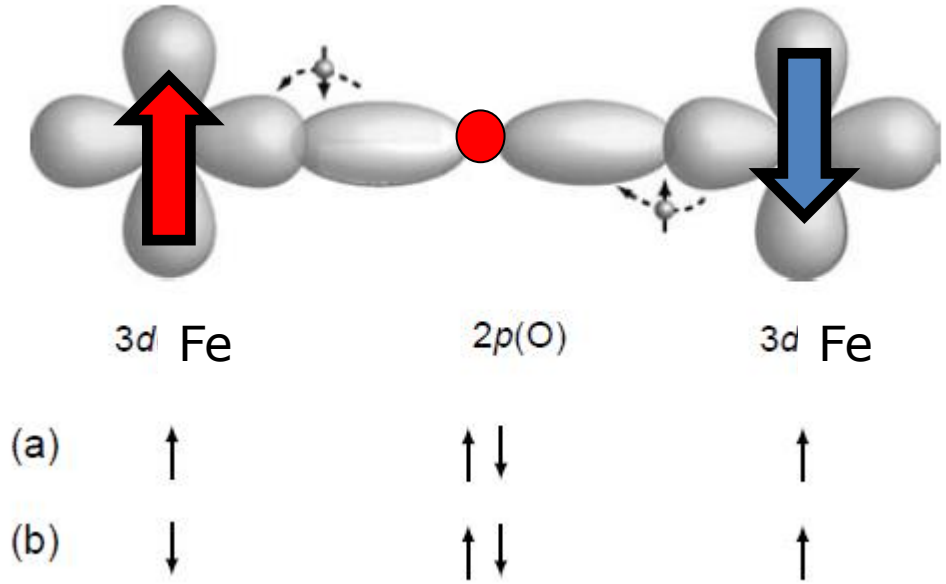
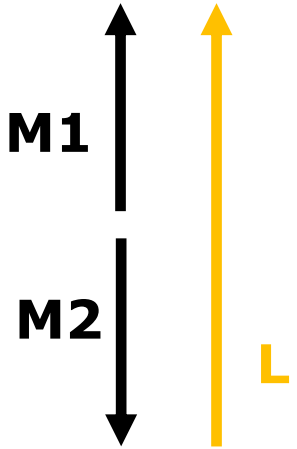
# Anti-Ferromagnetic Order, L

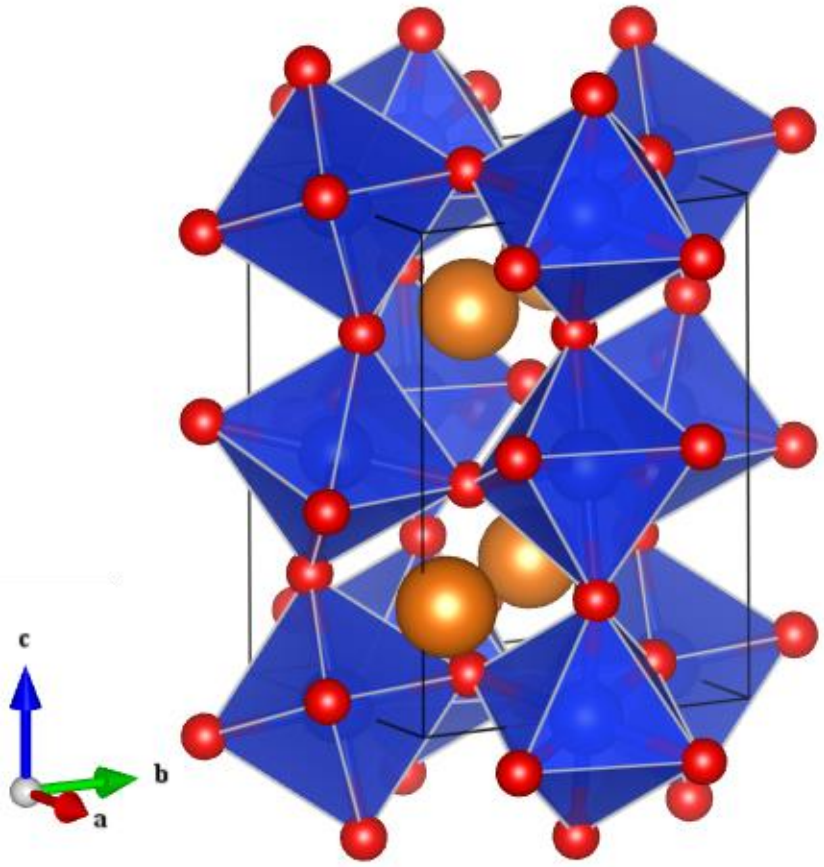


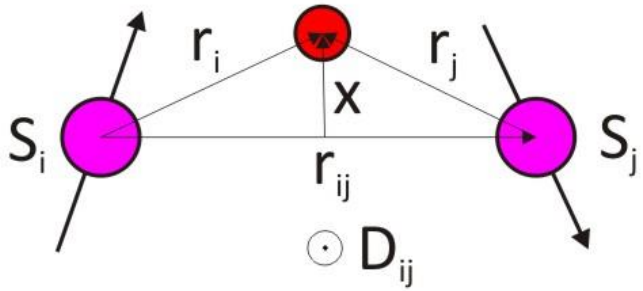




- Superexchange = electrons hop Fe – O – Fe
- Forbidden if spins are parallel
- Lower energy if spins are anti-parallel, two sub-lattices M1 and M2
- G-type anti-ferromagnetism = spin reverses along all cubic directions
- AFM vector L, along the line of spins

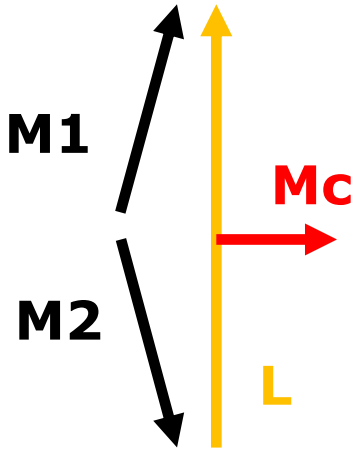


# Canted Magnetization, Mc



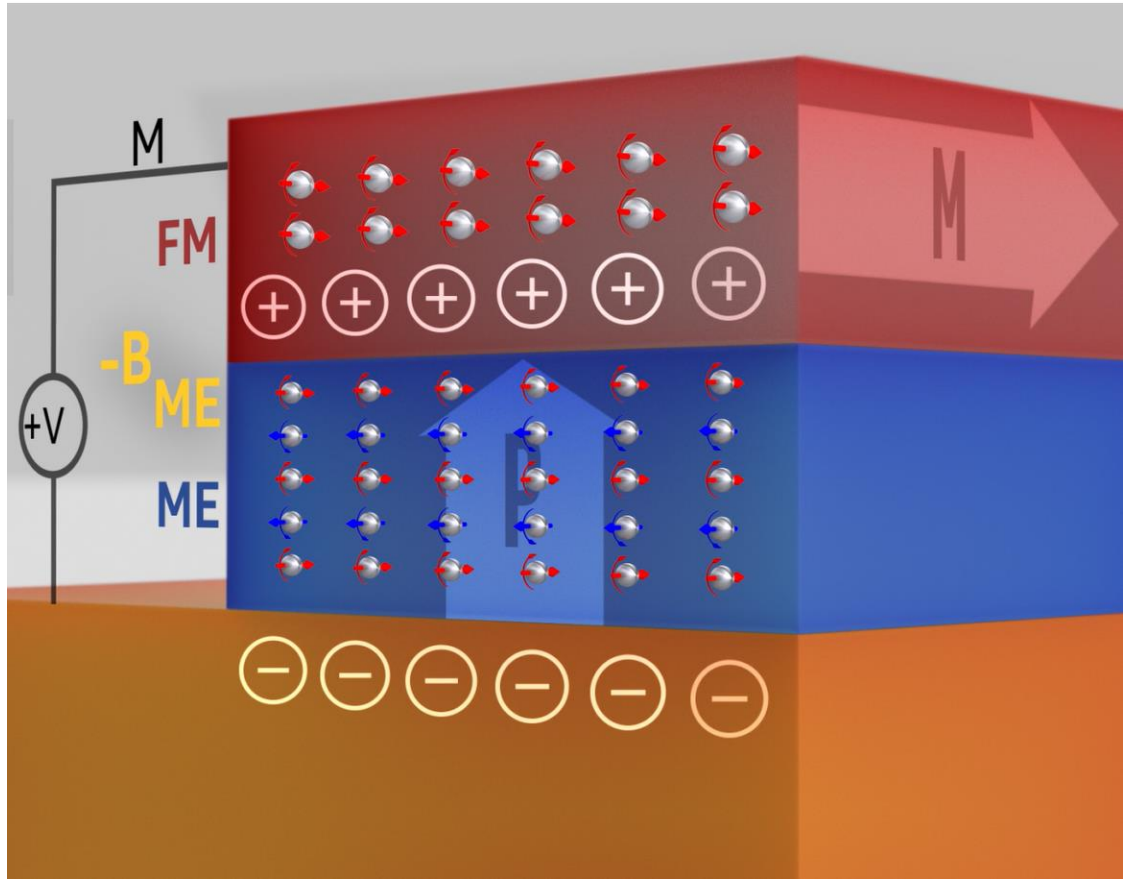




=P



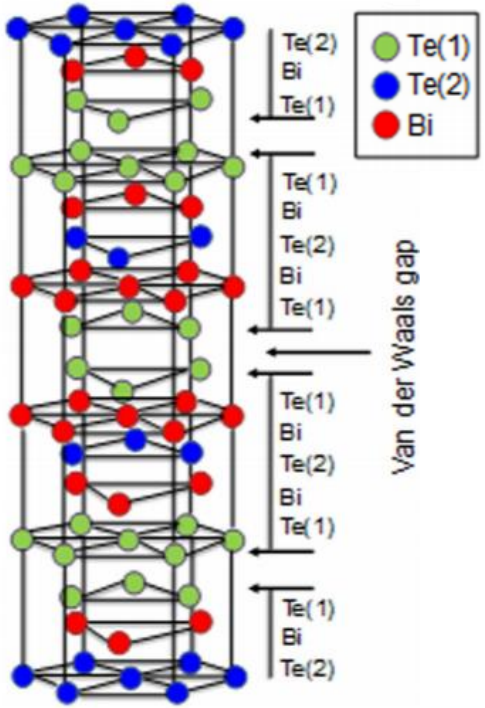

- Oxygen octahedra are not straight (Jahn-Teller distortion) but tilted
- If an oxygen is shifted from the straight line, modified exchange = Dzyaloshinskii-Moriya interaction (DMI)
- The two neighbor spins are not exactly opposite. Resulting "canted magnetization" Mc
- P, L, and Mc perpendicular to each other, right triple

# Magnetoelectric Switching

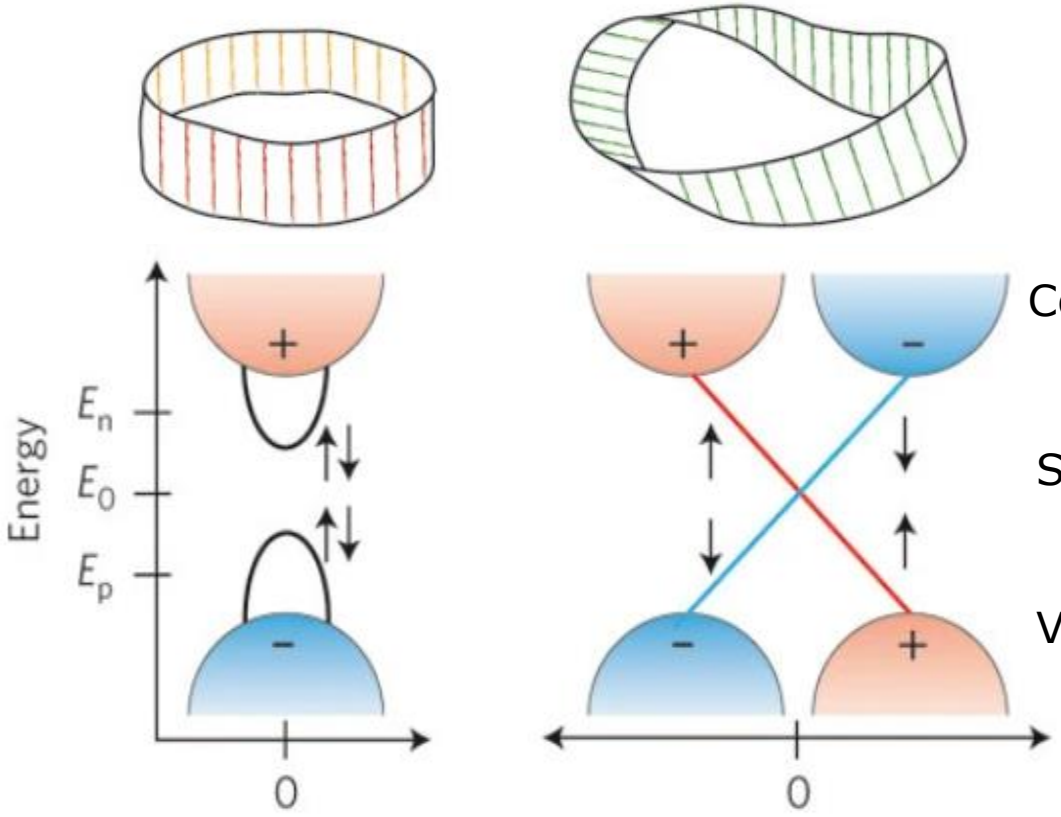



- Magnetoelectric effect = voltage-controlled switching of magnetization (charging a capacitor)
- More energy efficient than charge-controlled switching (spin torque)
- Magnetoelectric multiferroic, BiFeO3

# Topological Insulators




$Bi_2Te_3$
2D Layered TI




Typical Insulator



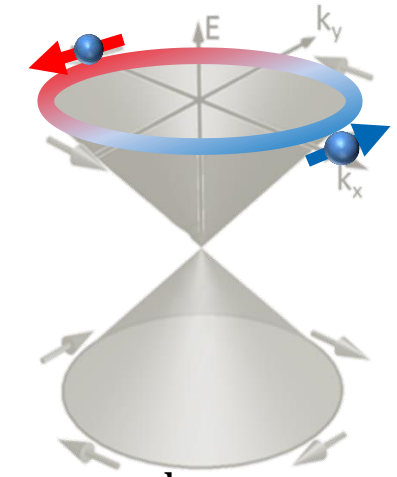

Topological Insulator

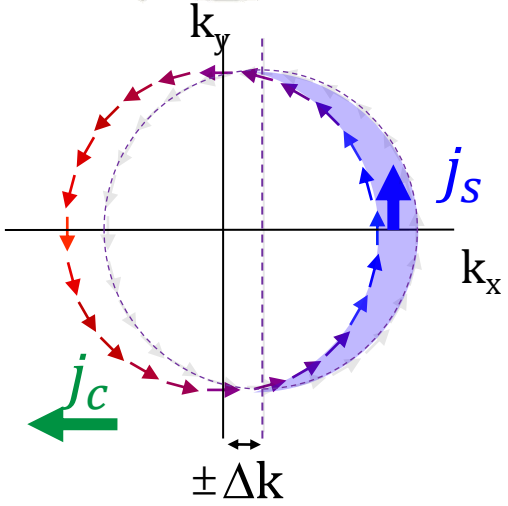
Topology
of Berry Phase

Conduction Band

Surface States

Valence Band

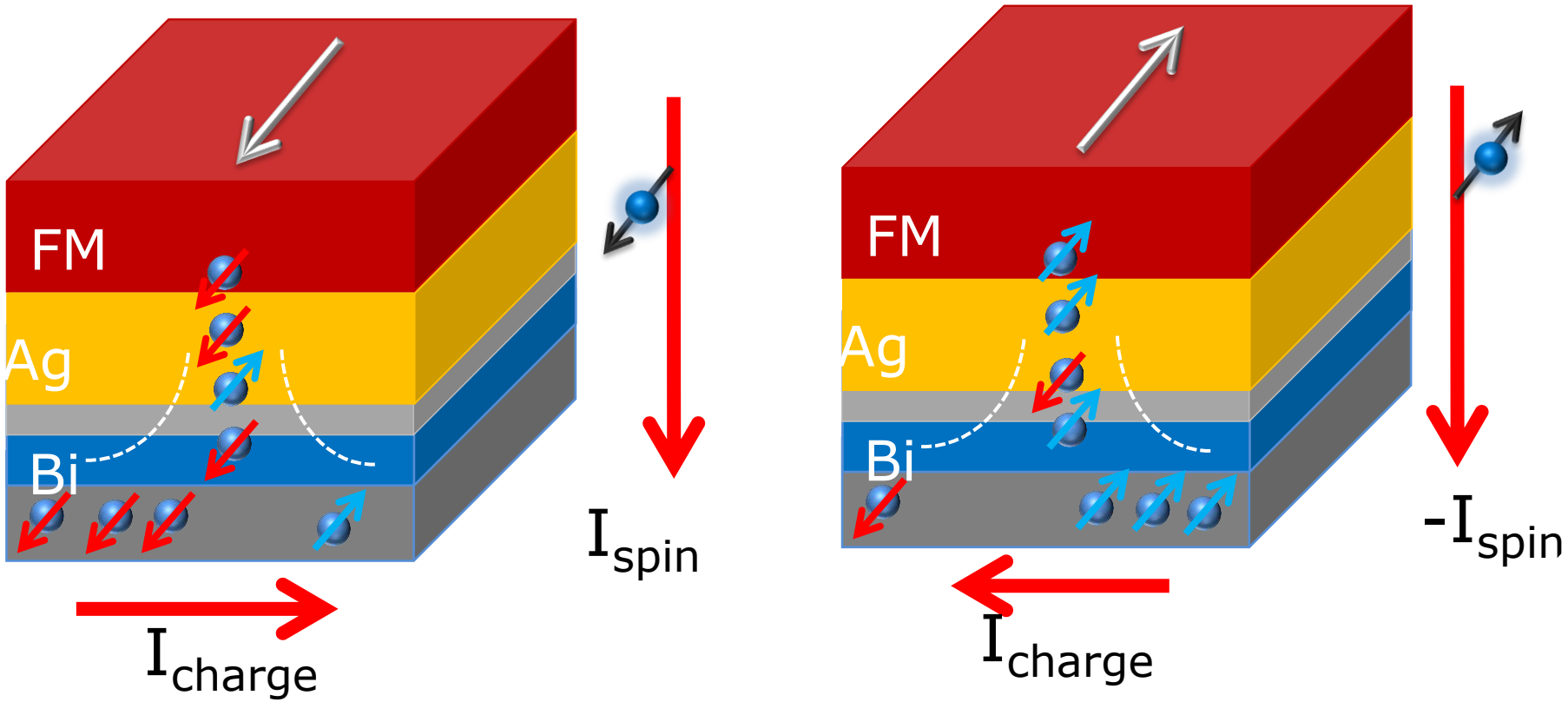



$$\theta_{soc} = \frac{j_s}{j_c}$$

**Large spin orbit coupling and inverted valence and conduction band states result in spin momentum locked surface states which have large $\theta_{soc}$.**

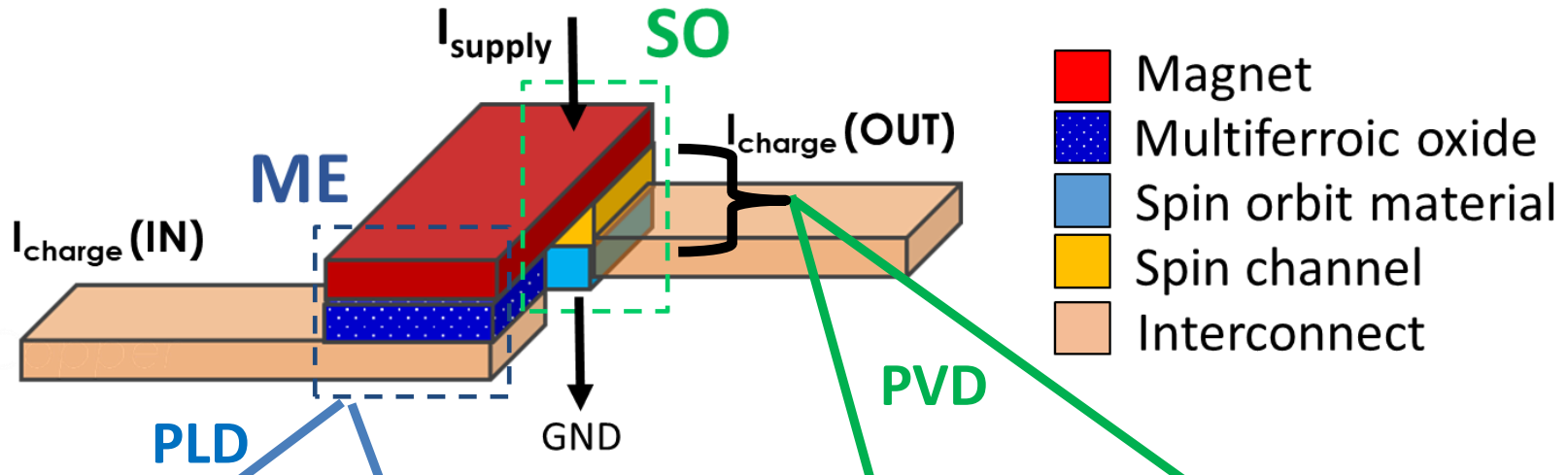
# Spin to Charge Conversion with Spin-Orbit



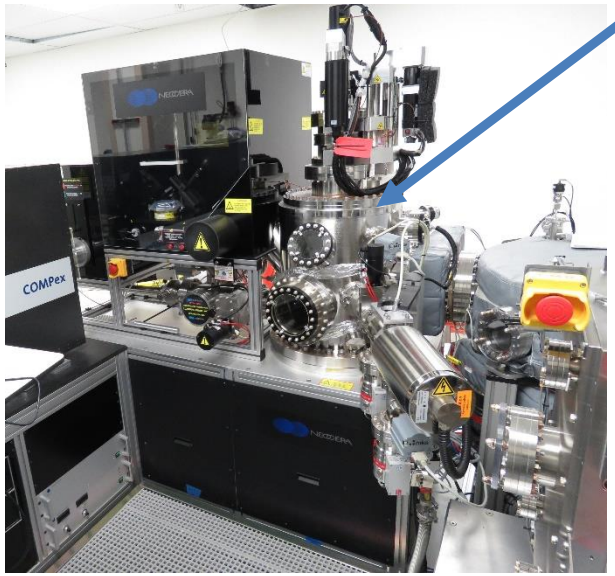

- High efficiency spin to charge conversion using spin orbit effects.
- Read off of the magnetization state.

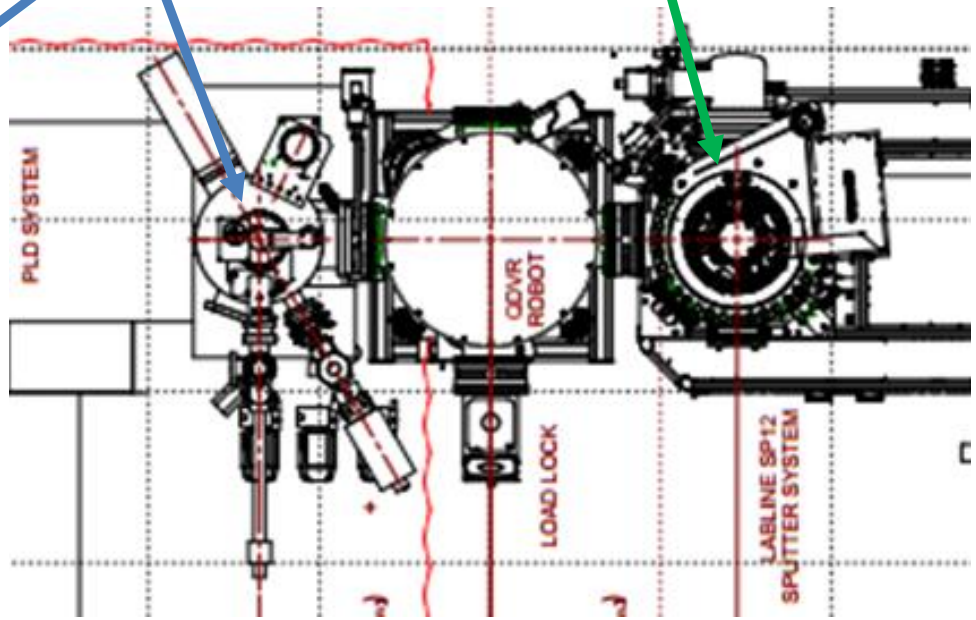
Edelstein, V. M. Solid State Commun. 73, 233–235 (1990)

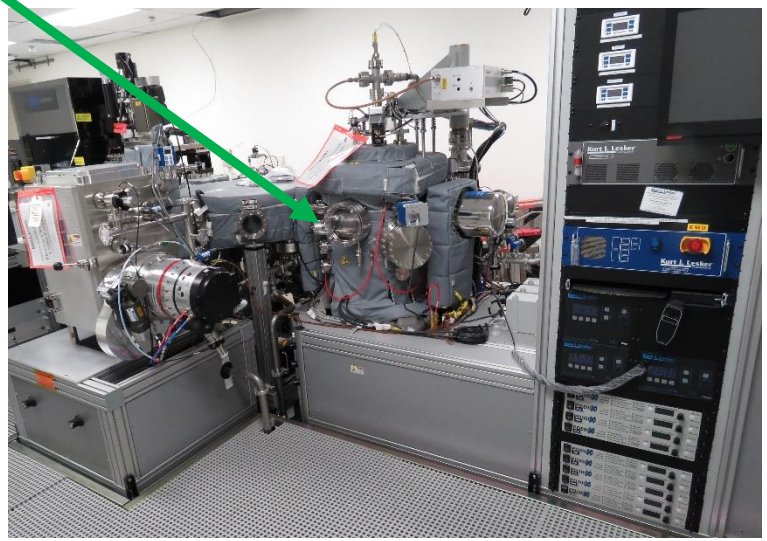
# ZPL90 in-situ deposition of Full MESO device stack: ME and SO Films




5

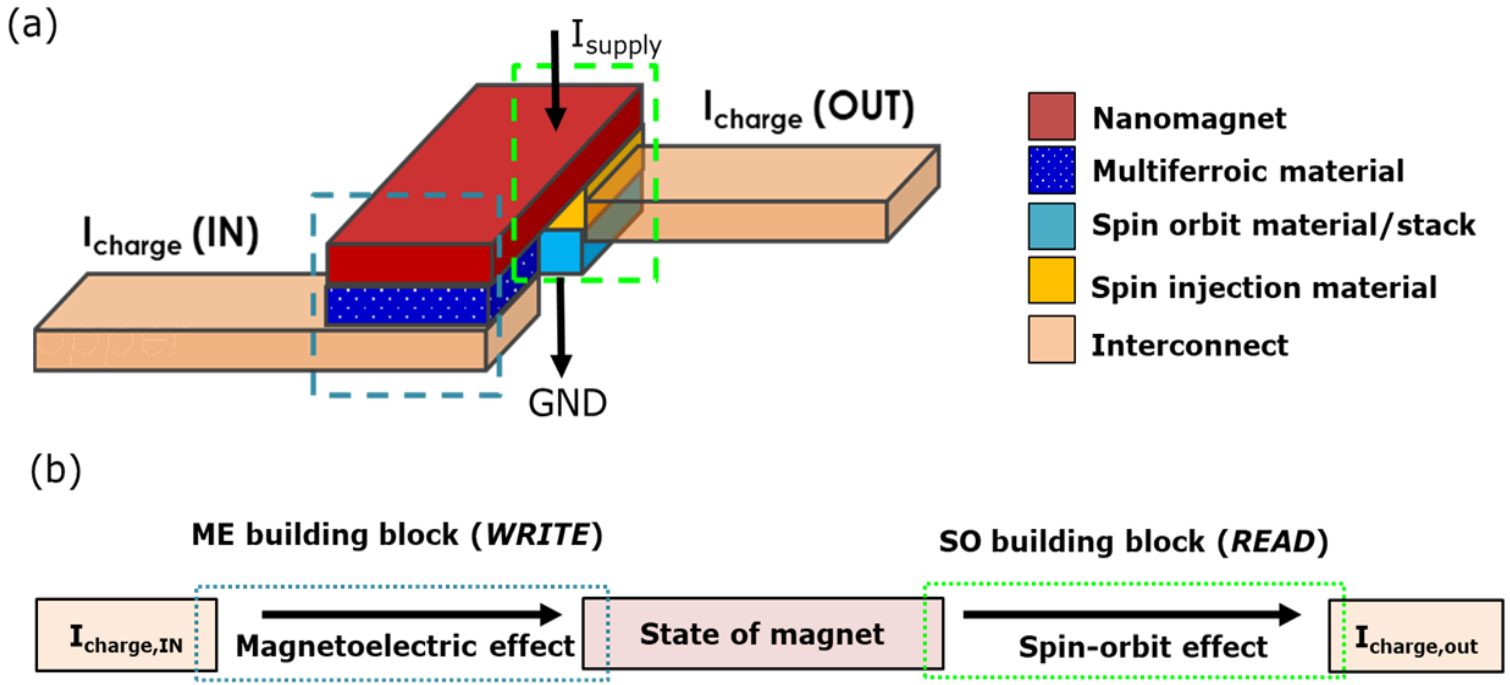


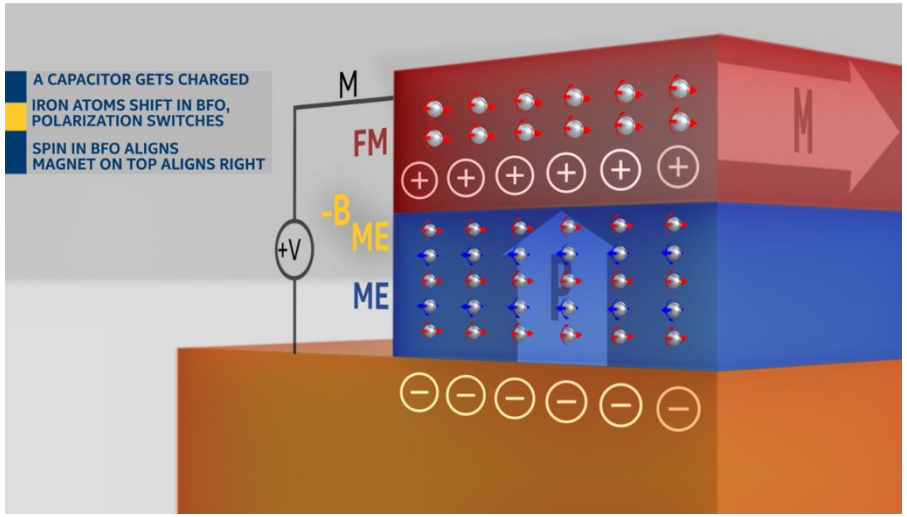



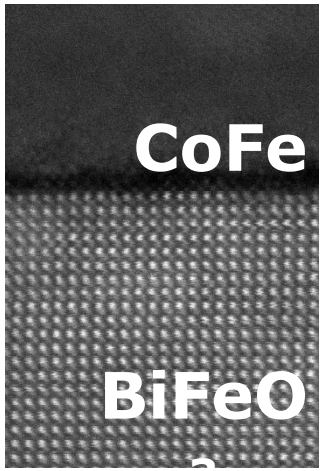



Multiferroic films (ME) in PLD chamber; magnet, heavy metal and TI films (SO) in PVD chamber

# Sub-100mV Logic Device Research Based On Magneto-Electric and Spin-Orbit Effects (MESO)



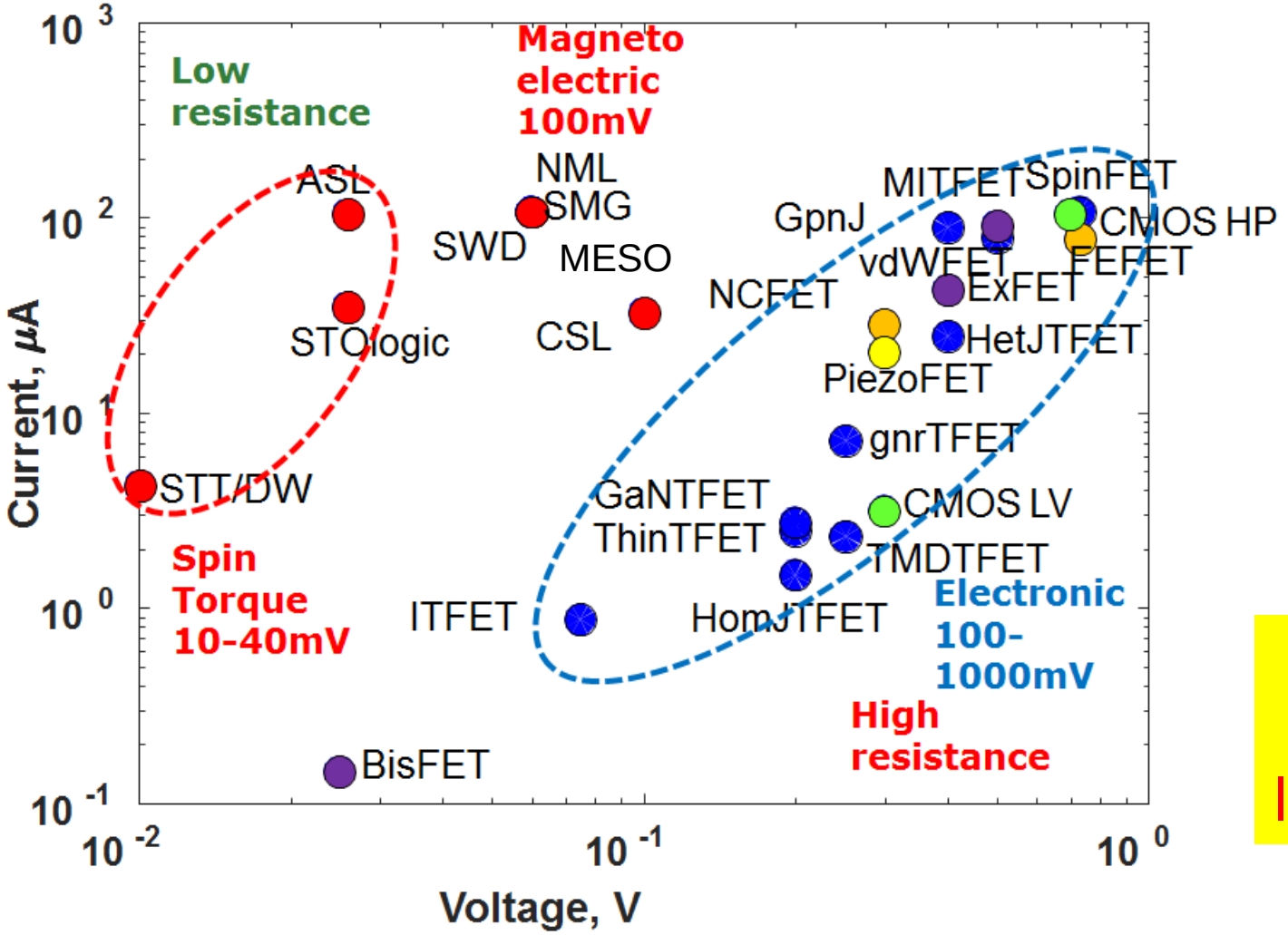



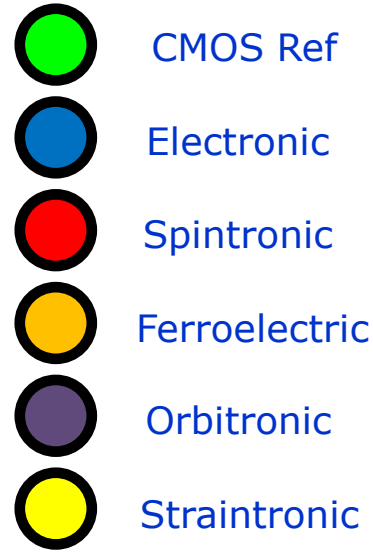




**MESO enables 4 CMOS nodes/generations of energy efficiency improvement same CMOS node.**


Ref. [1]: Intel Components Research, Nature 565 (7737), 35-42 (2018).
Ref. [2}: Intel Components Research, IEEE IEDM, pp. 37.3.1-37.3.4 (2019).

# Inputs to Benchmarking – Lower Voltage

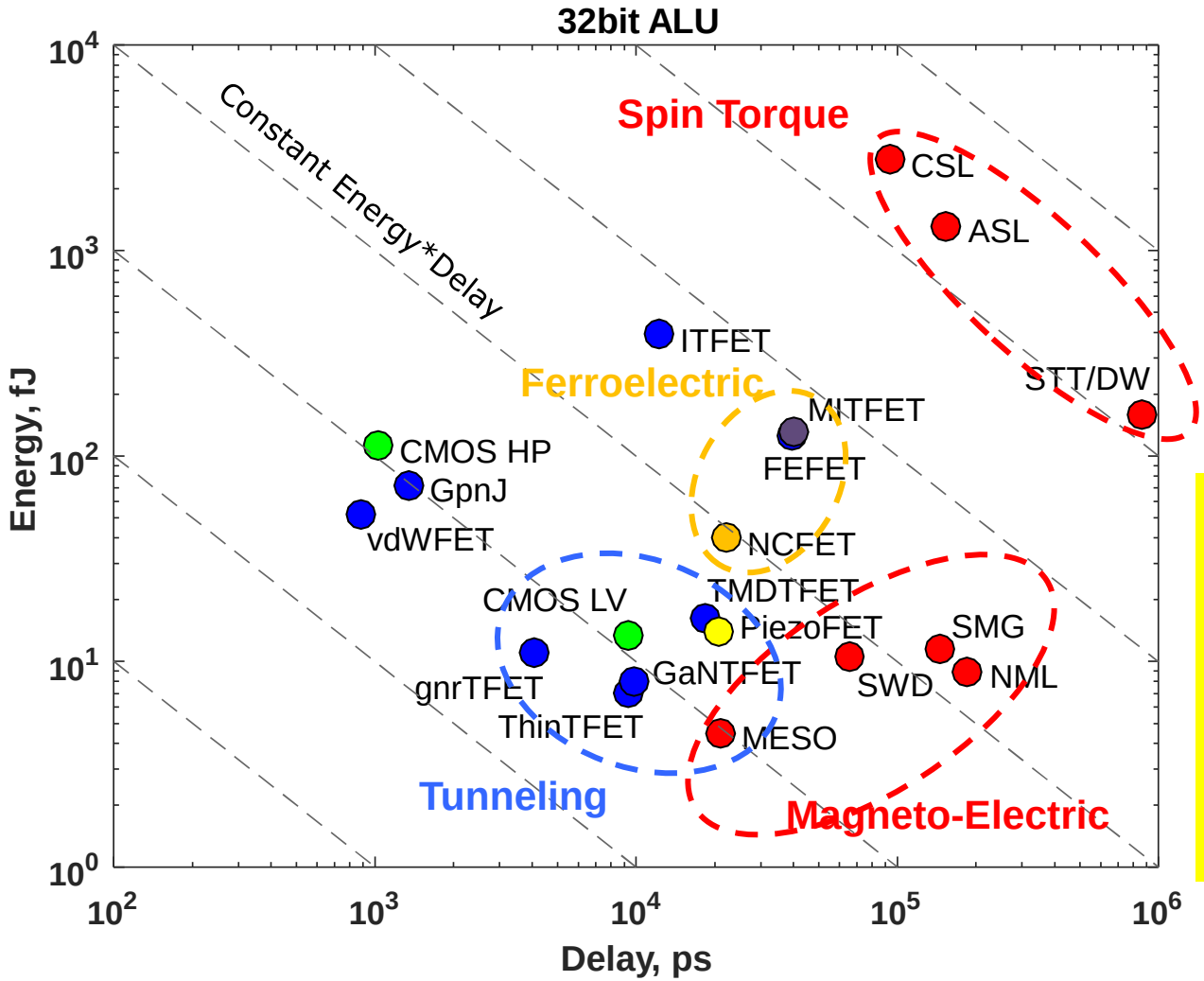



Spintronics enables lower voltage

*Ref: D. E. Nikonov and I. A. Young, IEEE JXCDC, vol. 1, pp. 3-11, Dec. 2015.*

# Lower Voltage = Best Path for Low Energy




CMOS Ref

Electronic

Spintronic

Ferroelectric

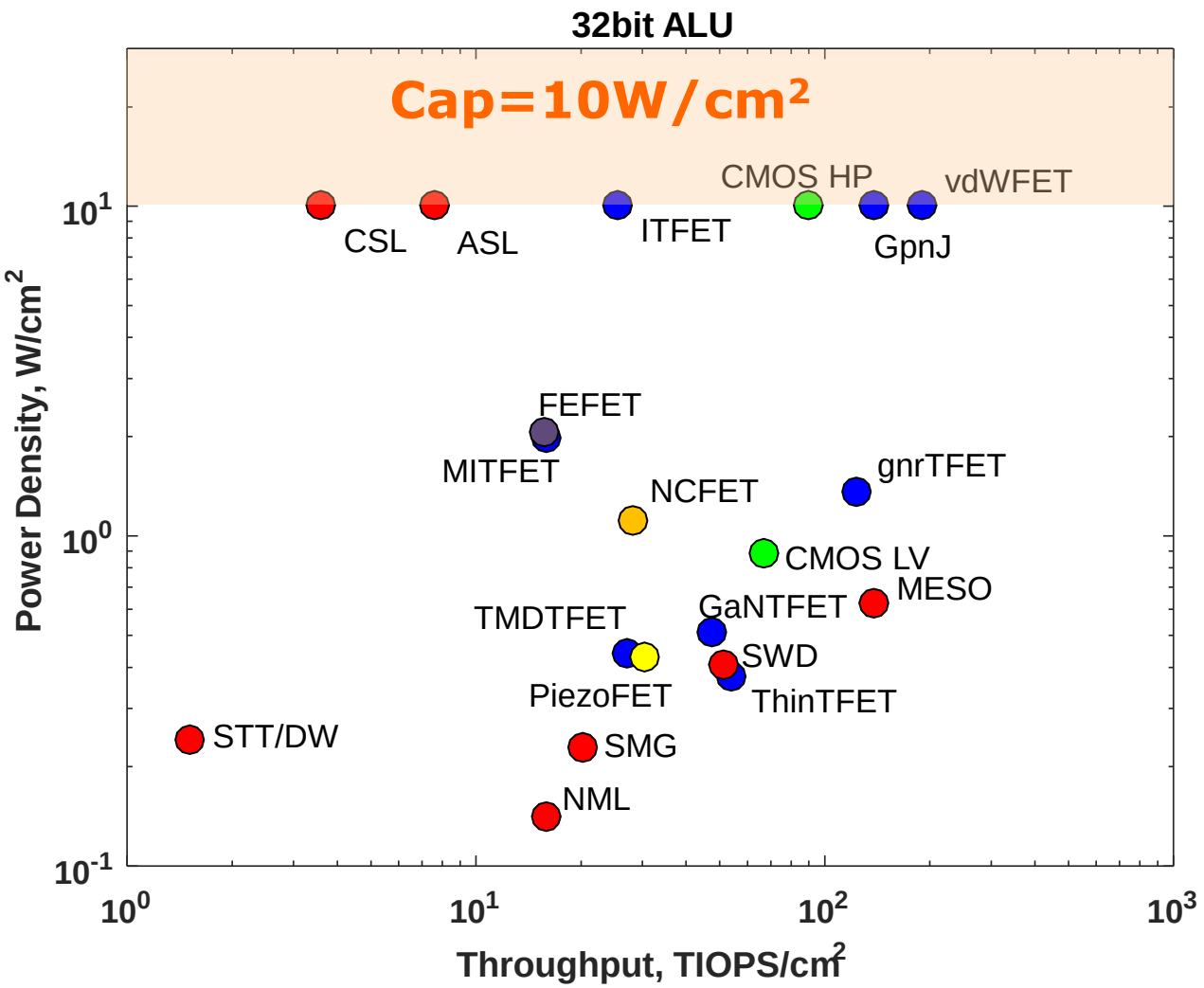
Orbitronic

Straintronic

**Tunnel FETs:**
Lower E*D than CMOS.

**Magnetoelectric Spintronics:**
Slower,
but lower energy; and
**Non-Volatile.**

# Throughput vs. Capped Power




- CMOS Ref
- Electronic
- Spintronic
- Ferroelectric
- Orbitronic
- Straintronic

**Tunnel FETs:**
Rival CMOS in throughput at lower power.

**Magneto-electric Spintronic:**
Very low power.

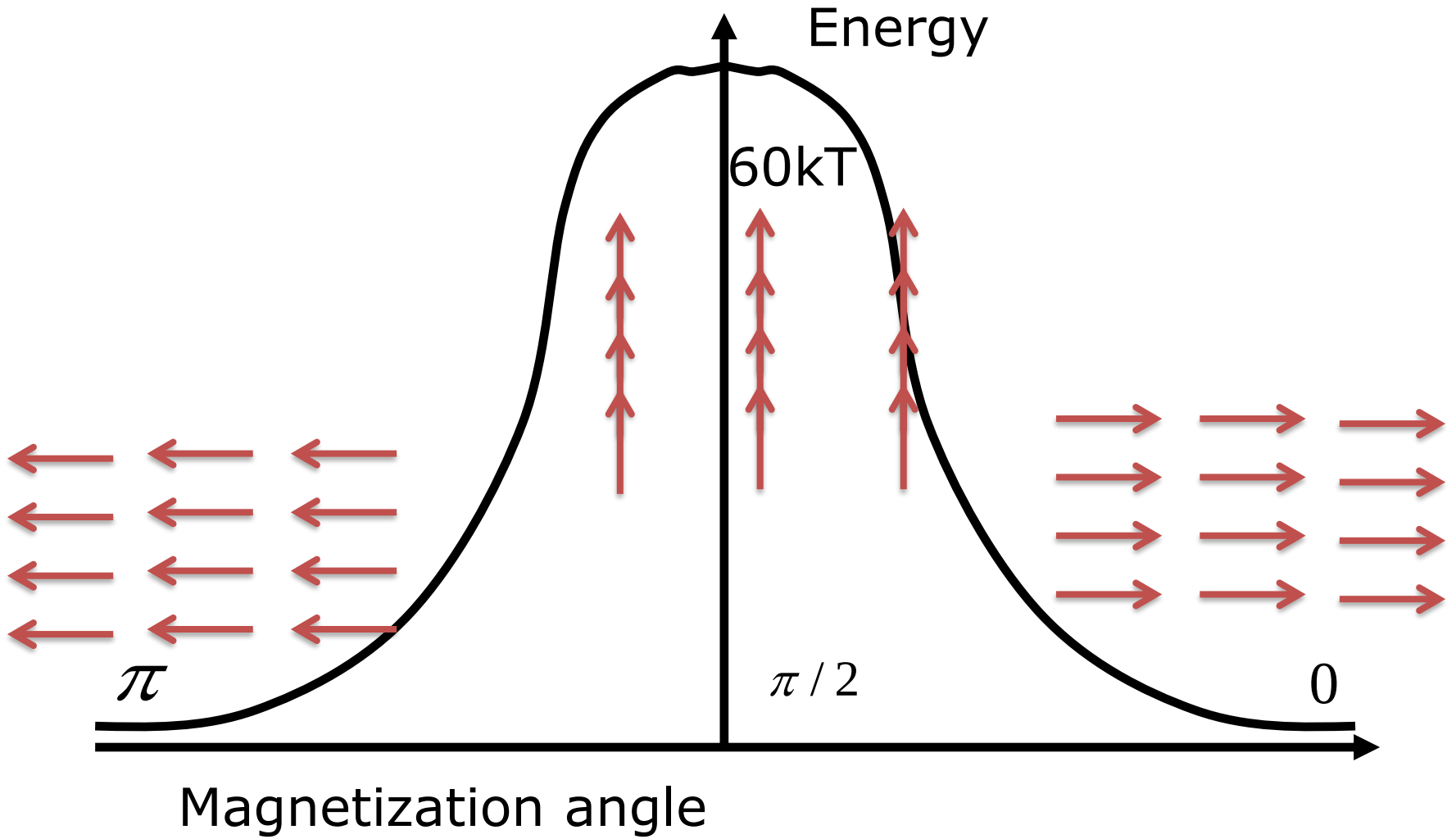
**TIOPS** = **T**era **I**nteger **O**perations **P**er **S**econd

# Take-Aways

- Moore's Law scaling of integrated circuits give exponential improvement of computing capacity but leads to the energy crisis
- Beyond-CMOS devices can switch at lower energy and promise the solution of the energy crisis
- Spintronics devices are based on spin torques
- Ferroelectric and multiferroic devices utilize lower energy switching of non-volatile order parameters
- Benchmarking of beyond-CMOS devices was developed and used for identifying promising devices, such as MESO

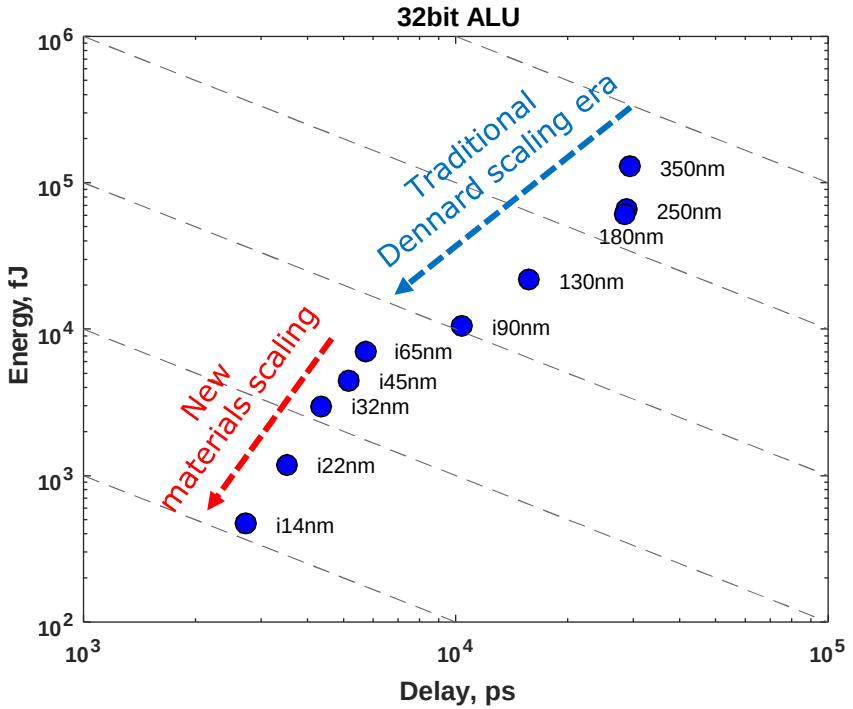
# BACKUP

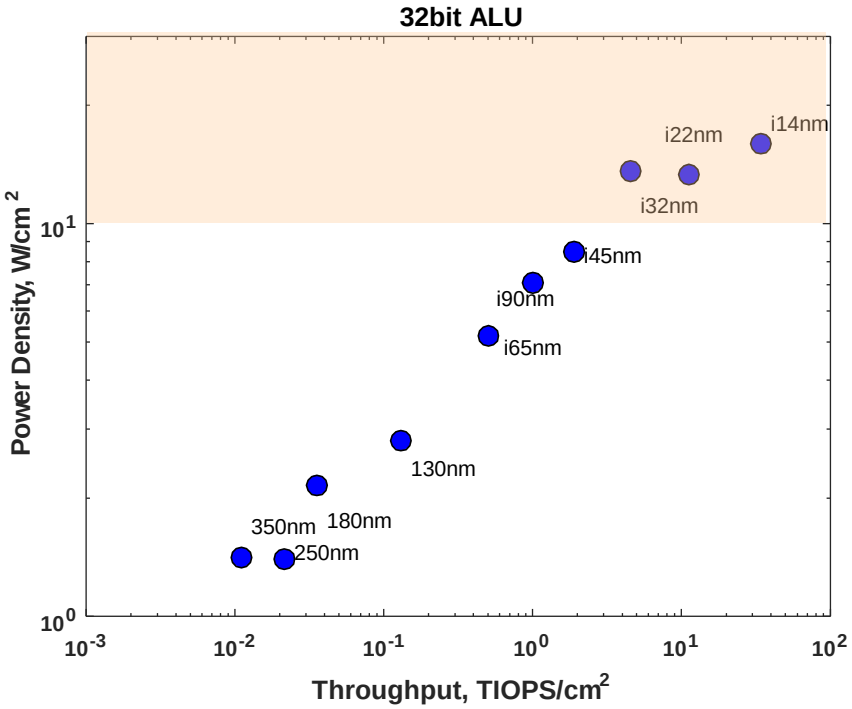
# Nanomagnet Energy Barrier




Energy barrier not lowered = reason for non-volatility

# CMOS Challenge With Energy



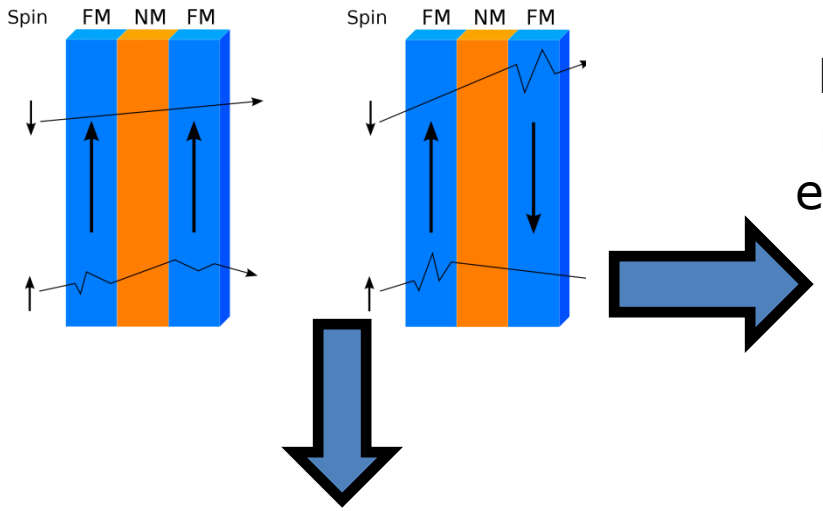




- As CMOS scales -> energy/op decreases.
- But energy/op not decreasing fast enough (for 2x increase transistors/cm$^2$)

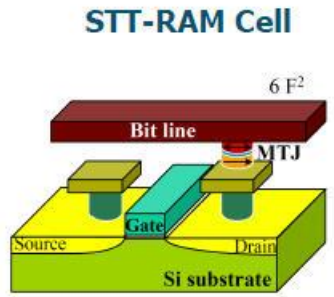
Power density approaches a Power Density constraint

* Source Intel: Projections based on best device data in papers published by Intel at IEDM in 1994 to 2014. Nikonov, Young, Benchmarking Method.

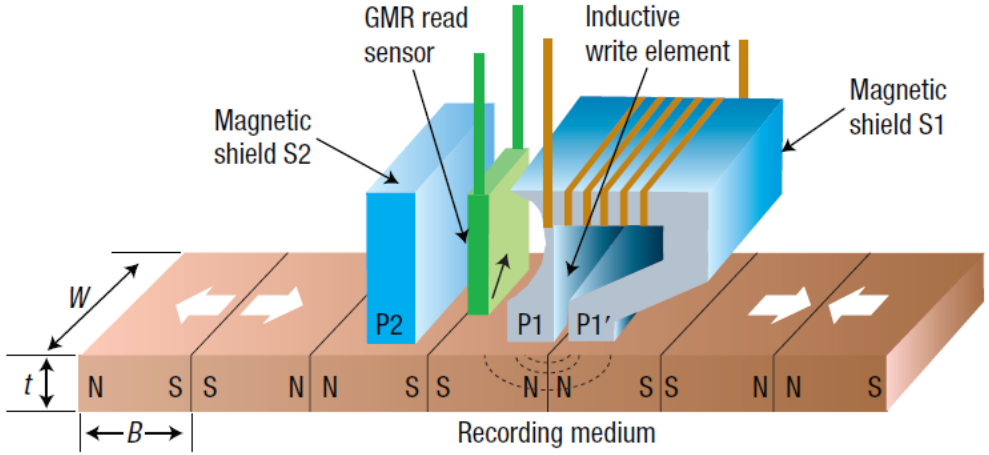
# Magnetoresistance and Its Uses



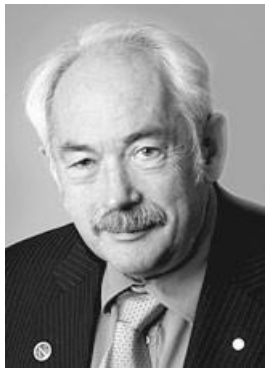

Magnetic memory, embedded?




1000x capacity of hard drives




A. Fert



P. Grunberg

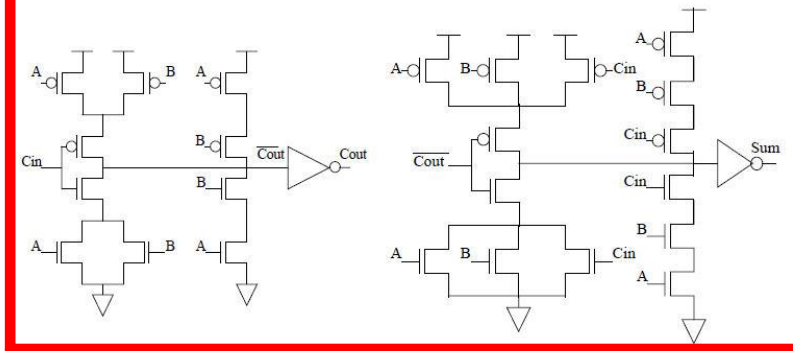

Nobel Prize 2007, physics

# Nomenclature of Beyond-CMOS Devices

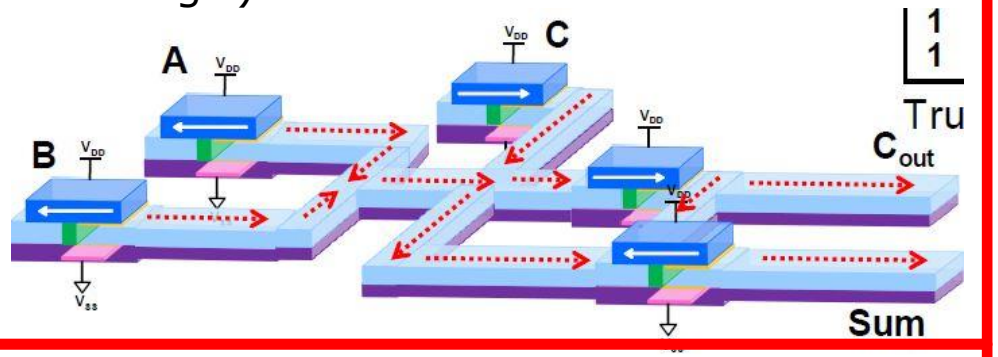
| Device name | acronym | input(s) | control | int. state | output | class | subclass |
|---|---|---|---|---|---|---|---|
| Si MOSFET high perf. | CMOS HP | V | Vg | Q | V | electronic | barrier |
| Si MOSFET low voltage | CMOS LV | V | Vg | Q | V | electronic | barrier |
| van der Walls FET | vdWFET | V | Vg | Q | V | electronic | barrier |
| Homojunction III-V TFET | HomJTFET | V | Vg | R | V | electronic | tunneling |
| Heterojunction III-V TFET | HetJTFET | V | Vg | R | V | electronic | tunneling |
| Graphene nanoribbon TFET | gnrFTET | V | Vg | R | V | electronic | tunneling |
| Interlayer tunneling FET | ITFET | V | Vg | R | V | electronic | tunneling |
| Two D Heterojunction Interlayer TFET | ThinFET | V | Vg | R | V | electronic | tunneling |
| GaN TFET | GaNFET | V | Vg | R | V | electronic | tunneling |
| Transition Metal Dichalchogenide TFET | TMDTFET | V | Vg | R | V | electronic | tunneling |
| Graphene pn-junction | GpnJ | V | Vg | R | V | electronic | refraction |
| Ferroelectric FET | FEFET | V | Vg | P | V | ferroelectric | hysteresis |
| Negative capacitance FET | NCFET | V | Vg | P | V | ferroelectric | non-hysteresis |
| Piezoelectric FET | PiezoFET | V | V | σ | V | straintronic | polarization |
| Bilayer pseudospin FET | BisFET | V | Vg | BC | V | orbitronic | exciton |
| Excitonic FET | ExFET | V | Vg | BC | V | orbitronic | exciton |
| Metal-insulator transistor | MITFET | V | Vg | Orb | V | orbitronic | bandstructure |
| SpinFET (Sughara-Tanaka) | SpinFET | V | Vg, Vm | Q, M | V | spintronic | spin drift |
| All-spin logic | ASL | M | V | M | M | spintronic | spin diffusion |
| Charge-spin logic | CSL | I | V | M | I | spintronic | spin Hall |
| Spin torque domain wall | STT/DW | I | V | M | I | spintronic | domain wall |
| Spin majority gate | SMG | M | V | M | M | spintronic | domain wall |
| Spin torque oscillator | STO | I | V | M | I | spintronic | nanomagnet |
| Spin wave device | SWD | M | I or V | M | M | spintronic | spin wave |
| Nanomagnetic logic | NML | M | B or V | M | M | spintronic | nanomagnet |

# Majority Gates = More Efficient Compute

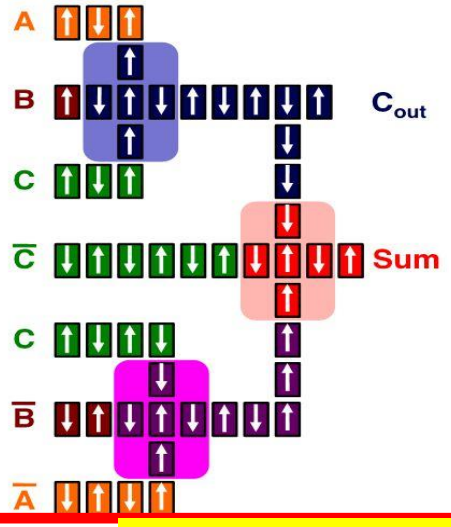
Adder = 28 transistors (at least)



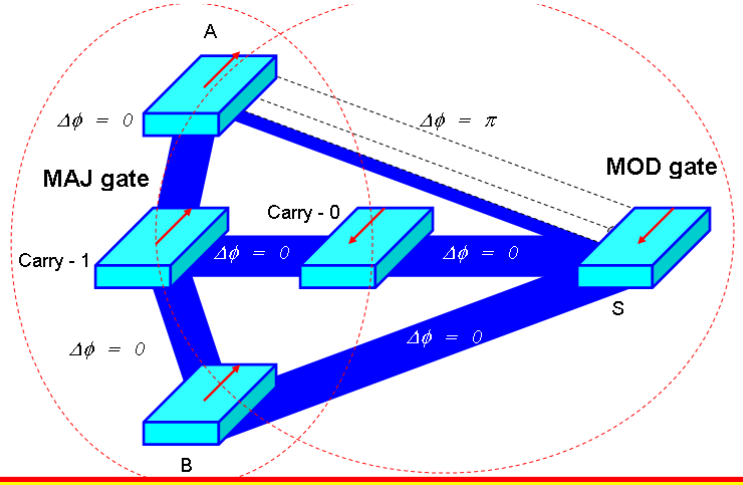

… or just 2 majority gates (All Spin Logic)




… or just 3 majority gates (Nanomagnetic Logic)

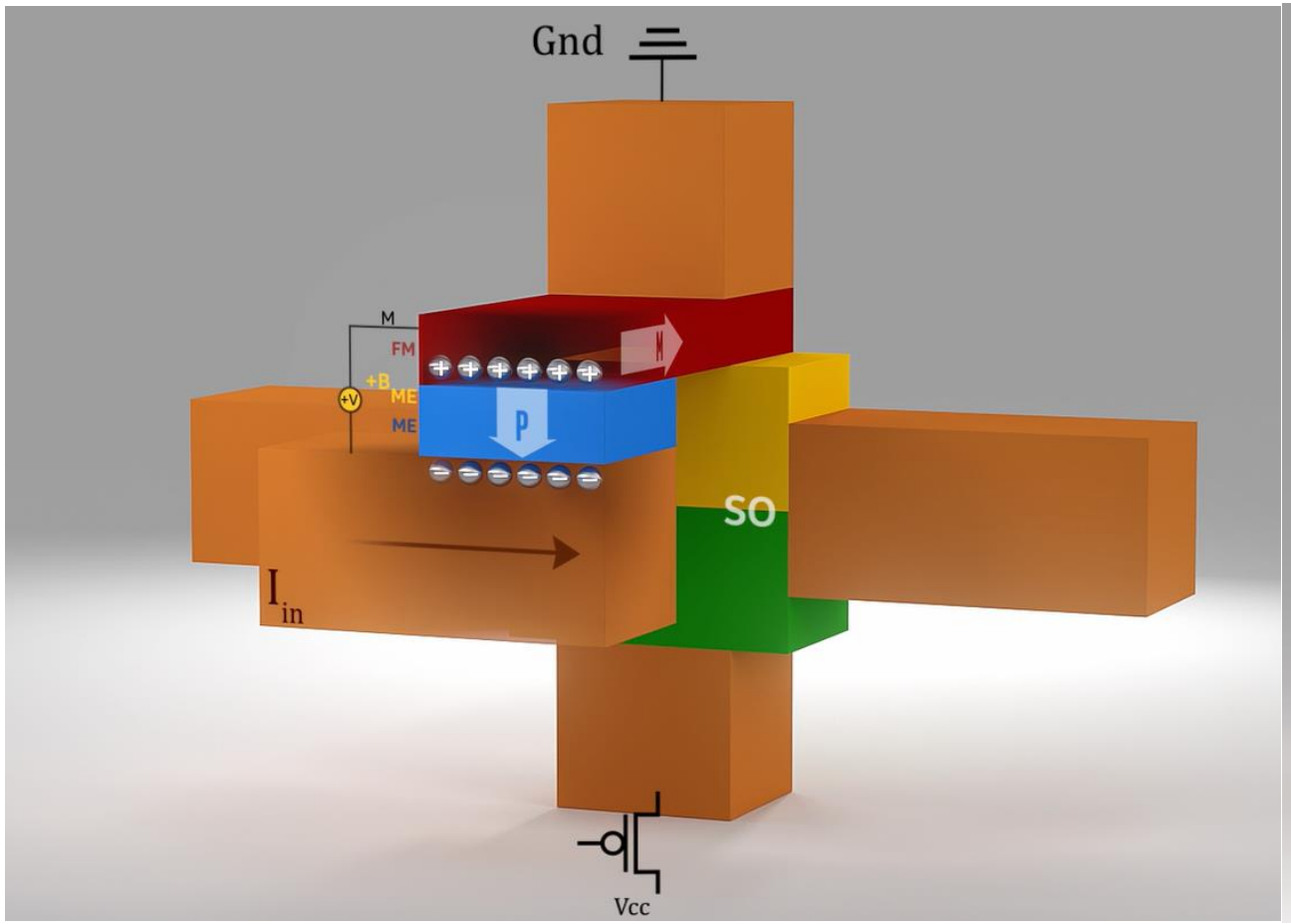


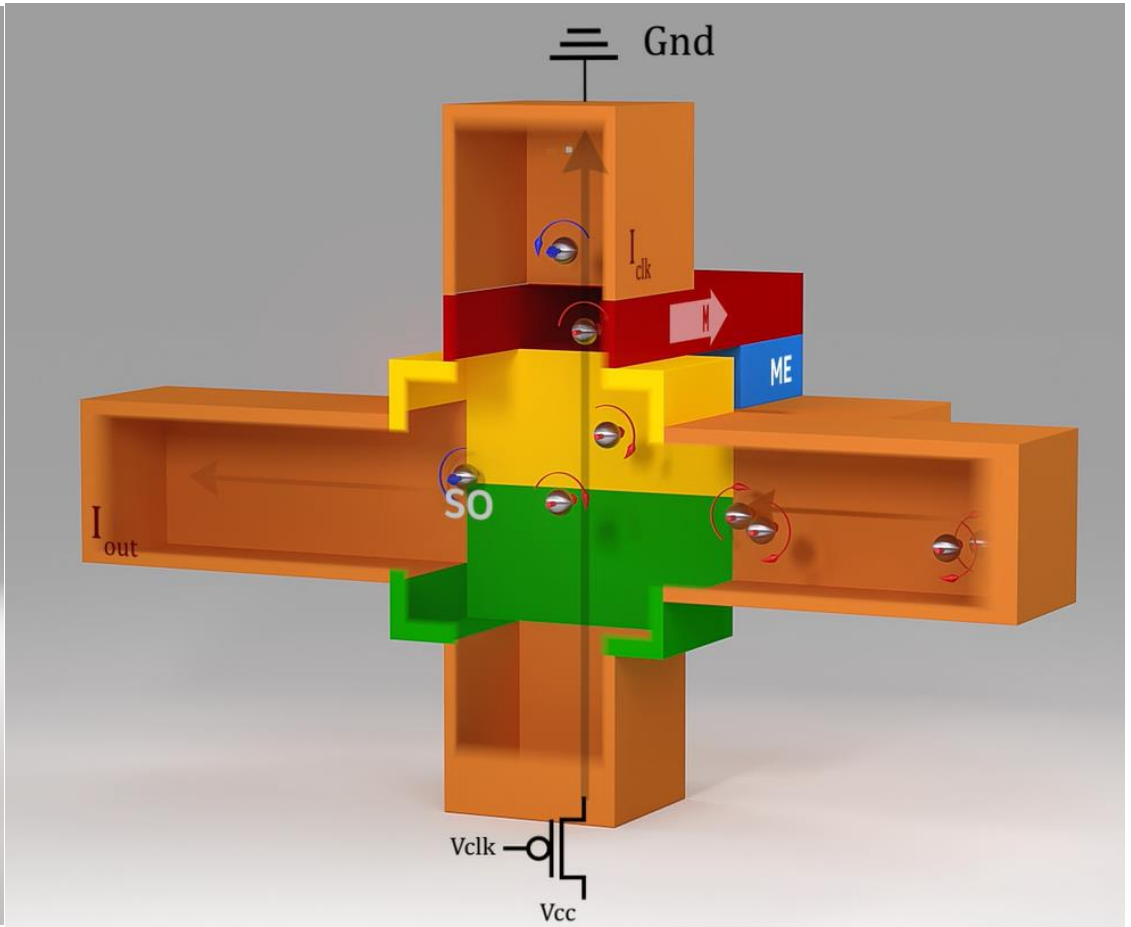

… or just 1 majority gate (Spin Wave Devices) !




Fewer devices for same computing function

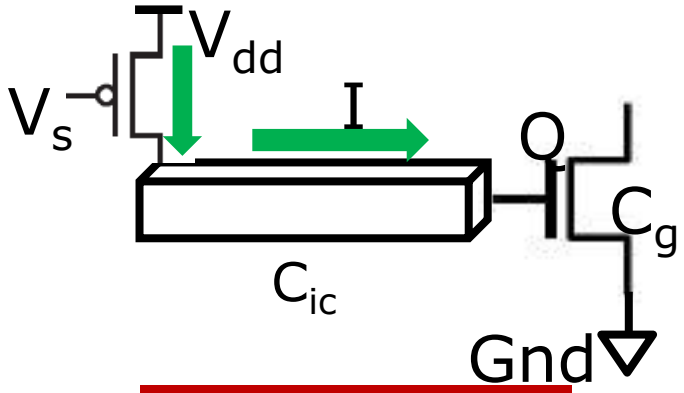
# Full MESO Operation Animation



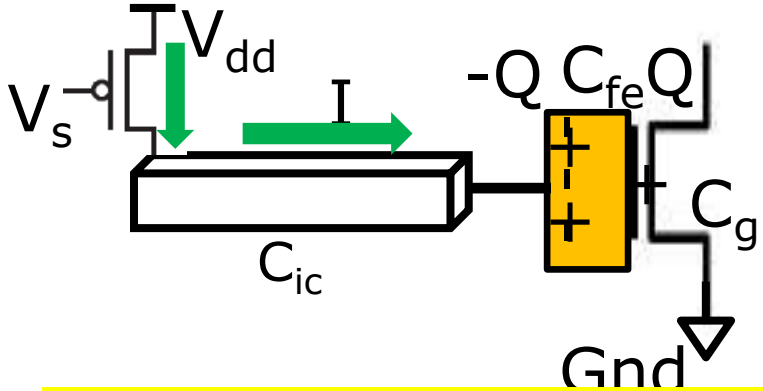



# Beyond-CMOS devices require CMOS

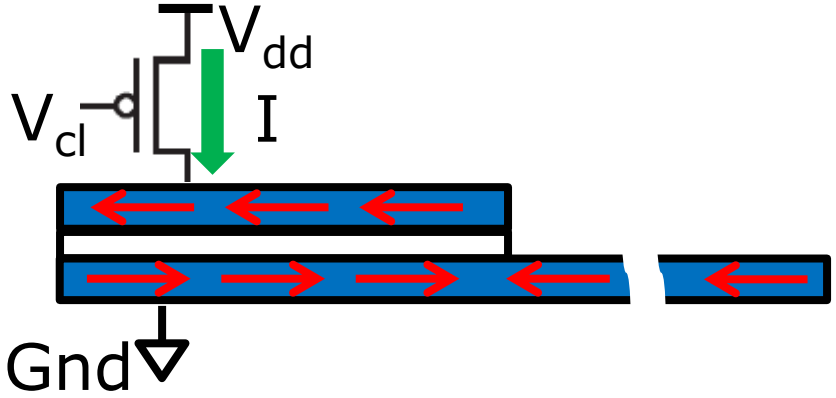
**A: Electronic**



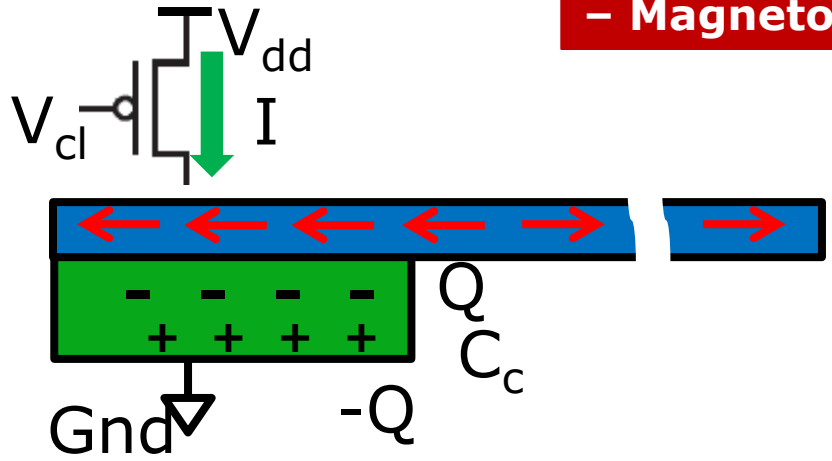

**B: Ferroelectric**




**C: Magnetic: Current driven - Spin Torque**



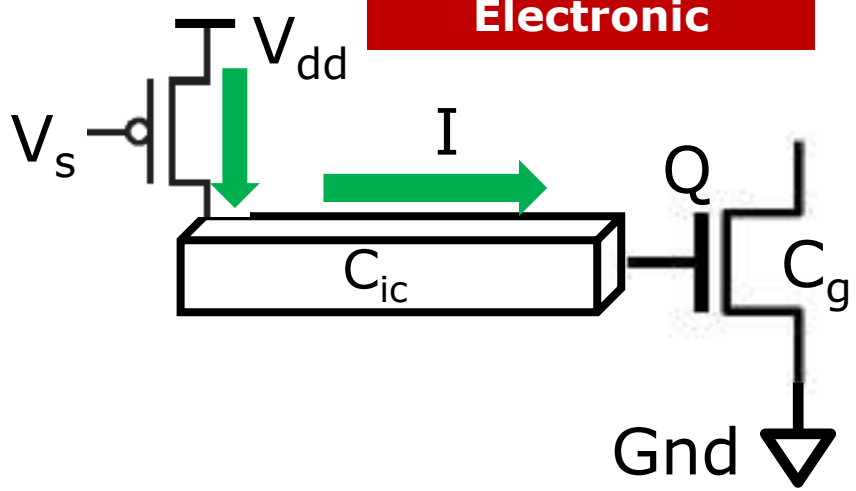

**D: Magnetic: Voltage driven – Magneto-Electric**




Contrary to concept of finding the next "switch" research

# Electronic vs. Ferroelectric Circuits

**Electronic**



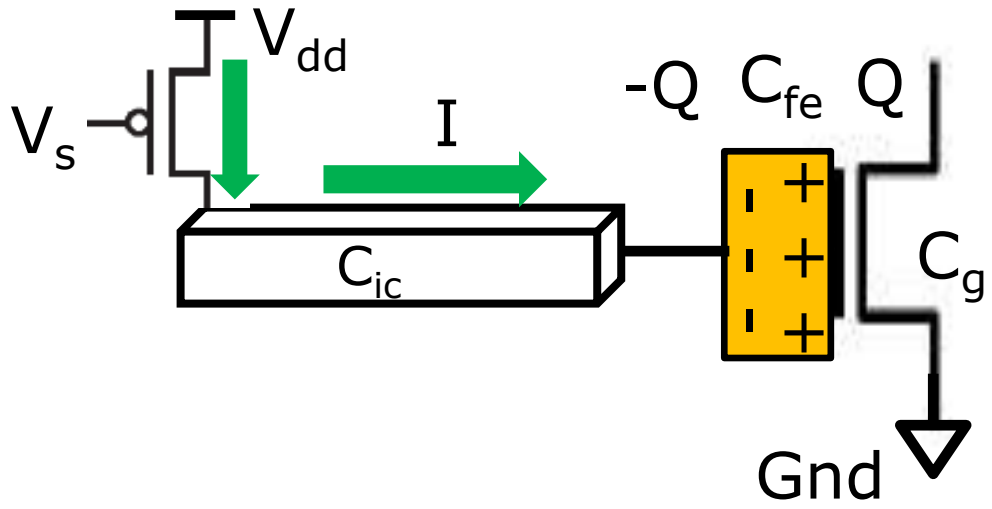

Switching time

$$t_{el} \approx CV_{dd}/I$$

Switching energy

$$E_{el} \approx CV_{dd}^{\ 2}$$

**Ferroelectric**




$$Q = P_{fe}A + CV_{dd}$$

Charging, intrinsic time

$$t_{ch} \approx Q/I$$

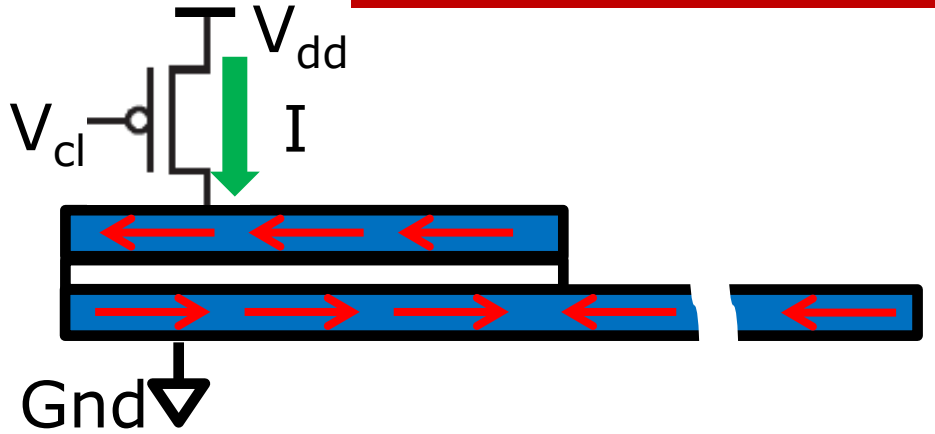
$$t_{fe} \approx 70\,ps$$

Switching energy

$$E_{fe} \approx QV_{dd}$$

# Spintronic Writing Circuits

## Current driven - spin torque



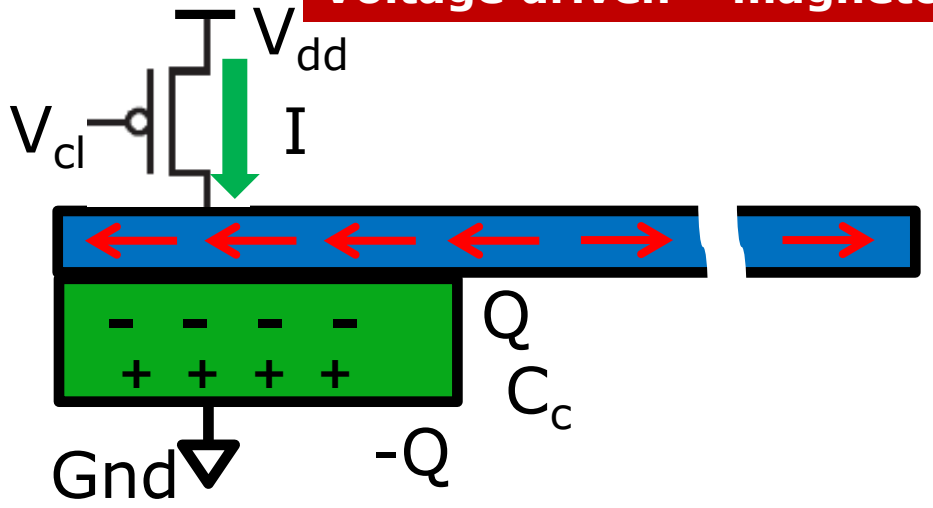

$$U_b = K_u v_{nm}$$ energy barrier

$$I_c = \frac{e\alpha U_b}{\hbar P}$$ critical current

$$t_{stt} = \frac{eM_s v_{nm}}{g\mu_B P(3I_c - I_c)} \log\left(\frac{2\pi\sqrt{2k_B T}}{\sqrt{U_b}}\right)$$

$$E_{stt} = I_{dev} V_{dd} t_{stt}$$

## Voltage driven – magnetoelectric




$$P_{ms} = \varepsilon_0 \varepsilon_{ms} \mathbb{E}_{ms}$$ polarization

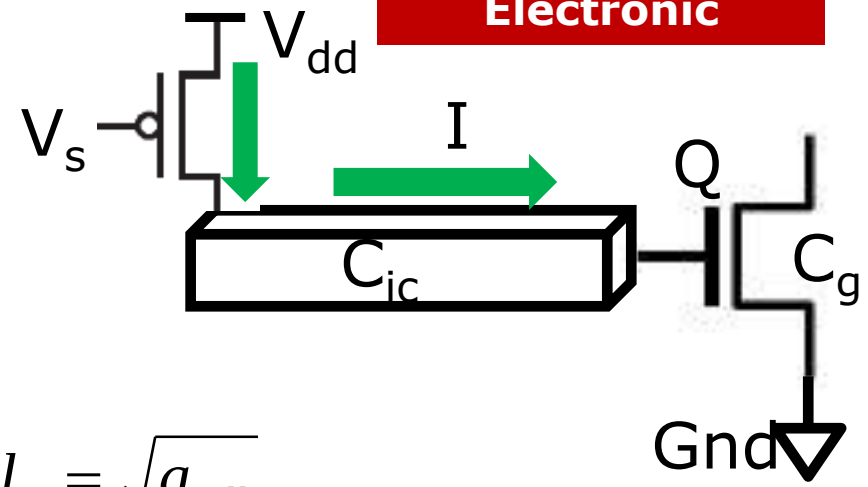
$$Q = P_s A + CV_{dd}$$ charge

$$t_{mag} = \frac{\pi}{2\gamma B_{me}}$$

$$E_{me} \approx QV_{dd}$$

# Treatment of Interconnects

**Electronic**




$$l_{ic} = \sqrt{a_{cell}}$$

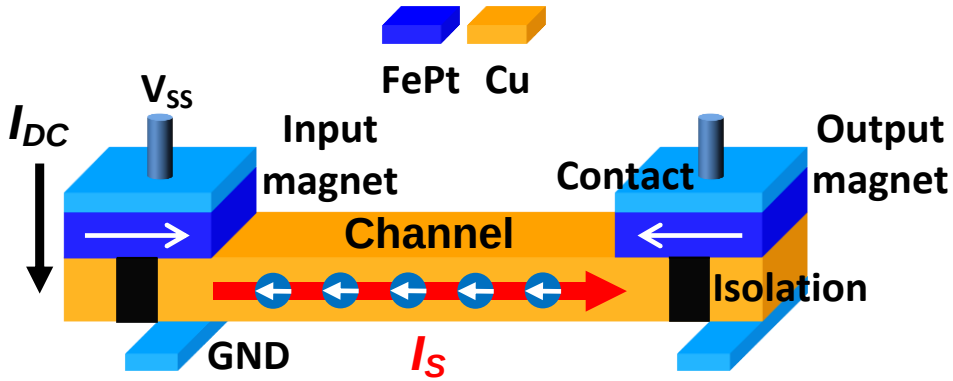
$$C_{ic} \approx l_{ic} \cdot 126aF/\mu m$$

$$t_{ic} \approx 0.7 C_{ic} V_{dd} / I$$

$$E_{ic} \approx 0.5 C_{ic} V_{dd}^{\ 2}$$

Neglecting resistance of wires

**Spintronic**




Cascaded nanomagnets for interconnects

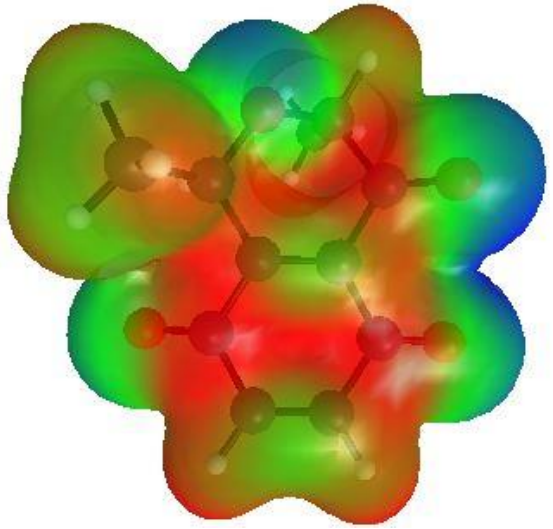
$$t_{ic} \approx t_{mag} + l_{ic}/c$$

Propagation delay

$$E_{ic} \approx E_{mag}$$

# Levels of Simulation

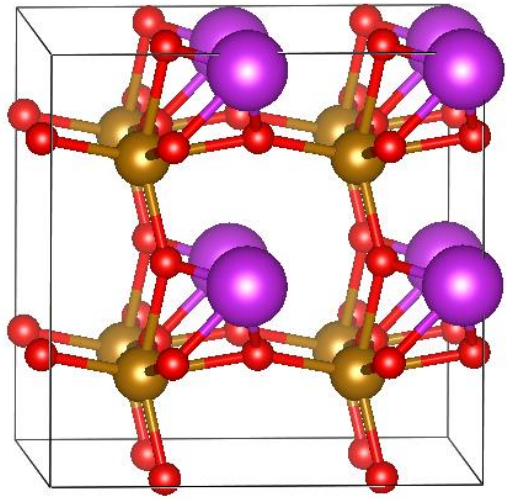
**1st principles**



**Many-body quantum mechanics. E.g. Density Functional Theory**

*Numerous tools*

**2nd principles**

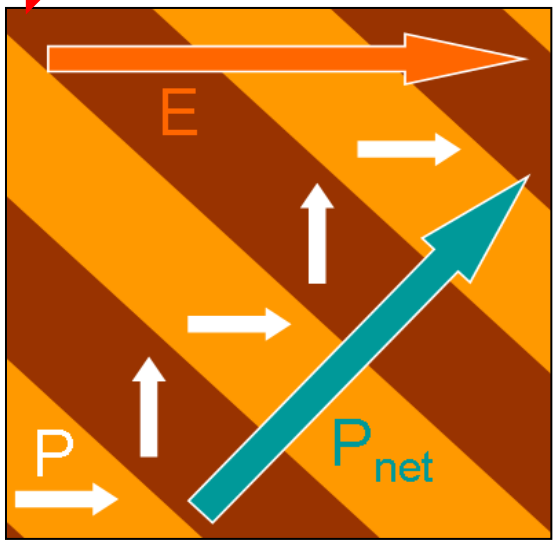


**Atomistic energies and coupling constants. E.g. Tight-binding**

*Prof. Iniguez (Luxembourg)*

Today

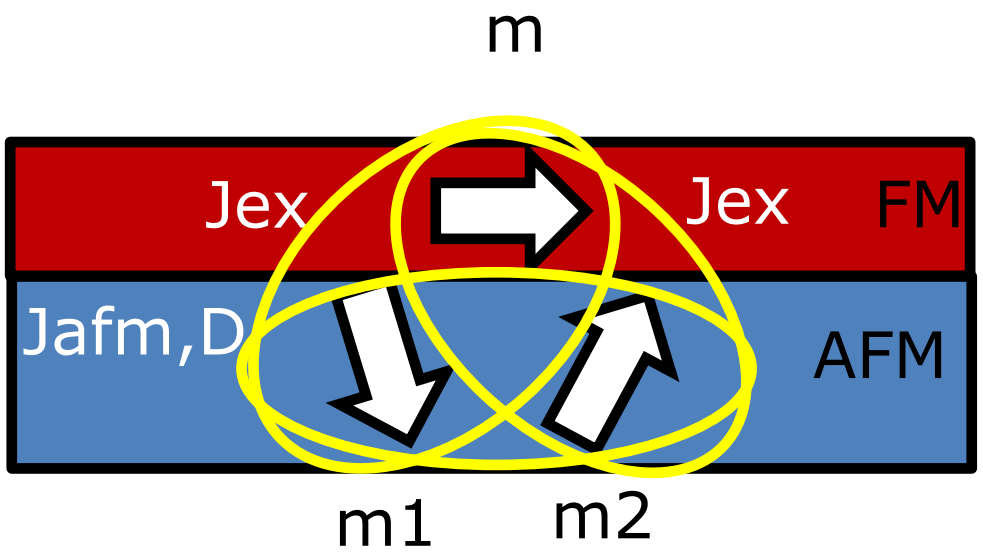
**3rd principles**




**Continuous medium. E.g. Landau-Khalatnikov eqs.**

*Intel*

# Surface Exchange In the Heterostructure




Macrospin (i.e. no spatial variation, no exchange stiffness)
All m are unit vectors. The two sublattices equivalently described:

$$L = \frac{\hat{m}_1 - \hat{m}_2}{2}$$

$$M_c = \hat{m}_1 + \hat{m}_2$$

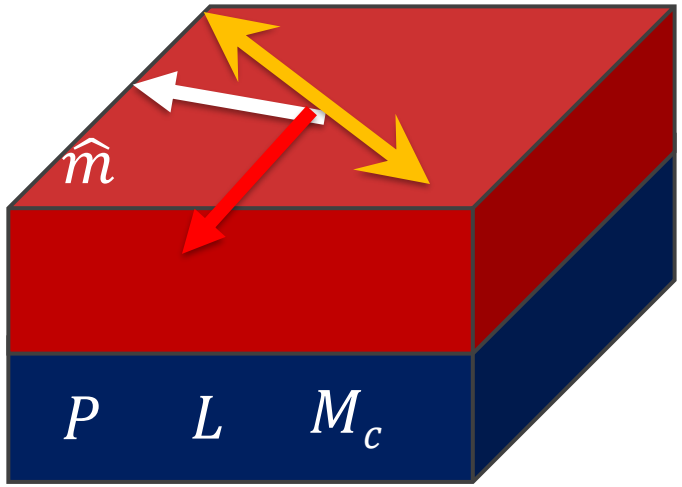
$$\hat{m}_1 = L + M_c / 2$$

$$\hat{m}_2 = -L + M_c / 2$$

# Exchange Bias and Exchange Coupling

$\vec{H}_{eff}(\vec{L})$

FM, CoFe




$\vec{H}_{eb}$

Multiferroic, BFO

$$F_{FM-AFM} = M_{fm} H_{eb} \left(\hat{m}_c \cdot \hat{m}\right) - \frac{M_{fm} H_{ec}}{2} \left(l \cdot \hat{m}\right)^2$$

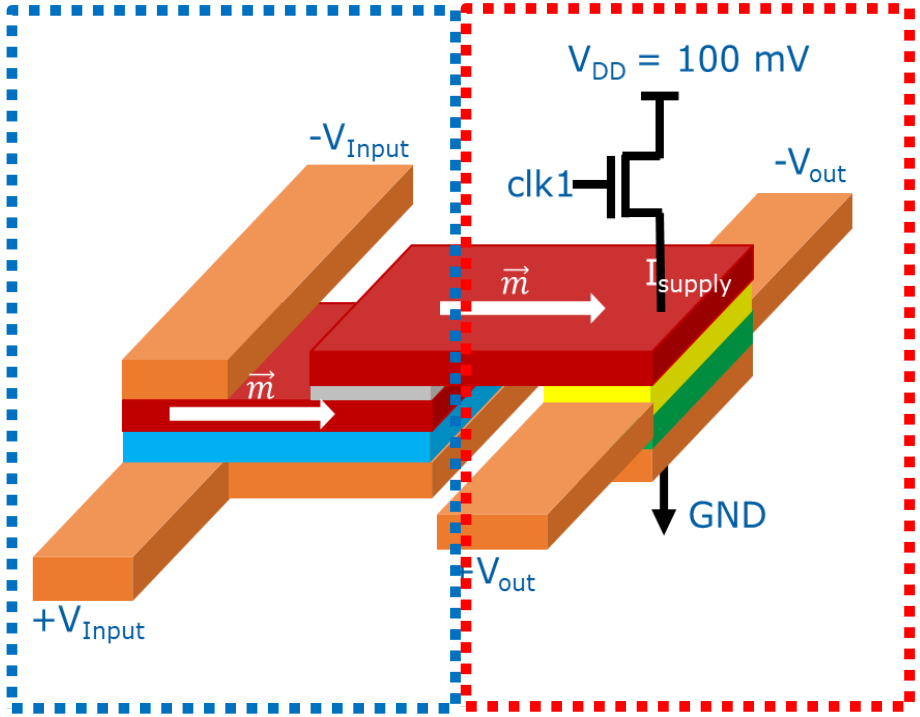
**Exchange bias**
Acts are field along
CANTED MAGNETIZATION (Mc)

**Exchange coupling**
Acts as easy axis anisotropy along
ANTIFERROMAGNETIC (L)

# Magneto-Electric Spin-Orbital (MESO) Device

Magnetoelectric (ME) input

Spin-Orbital (SO) output

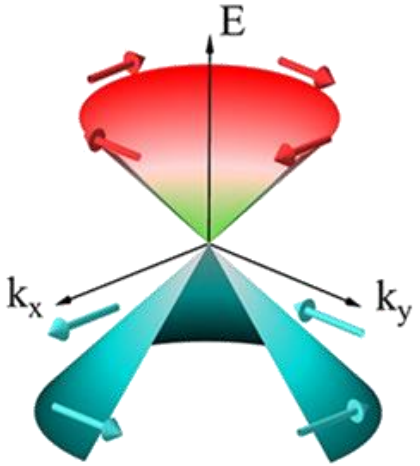


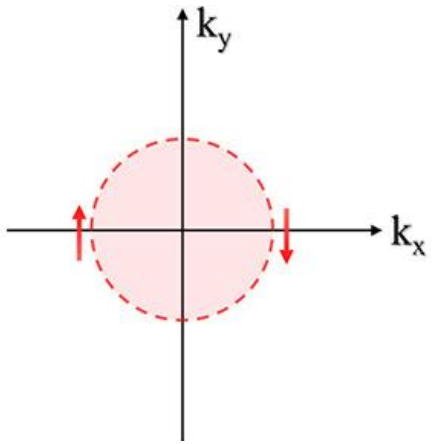

- The way to lower switching energy $E \sim CV^2$, is lowering voltage
- 12 years of research in the Semiconductor Research Corporation (SRC)
- Magnetization switching can be done at lower voltage (~0.1V)
- Non-volatility of logic = built-in registers and latches = added benefit

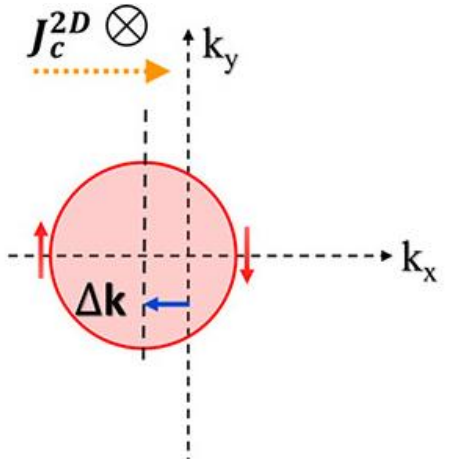
S. Manipatruni et al., Nature 565 (7737), 35-42 (2019).

# Insert's effect on spin to charge conversion efficiency

Topological Insulator

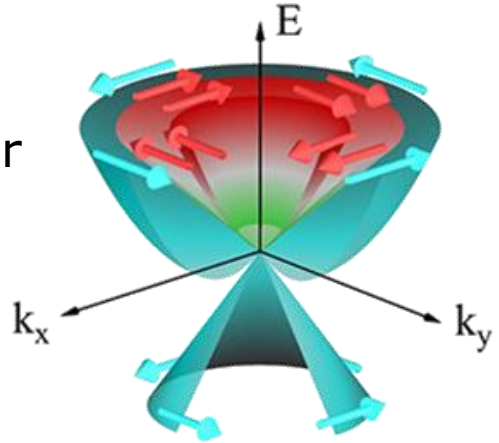


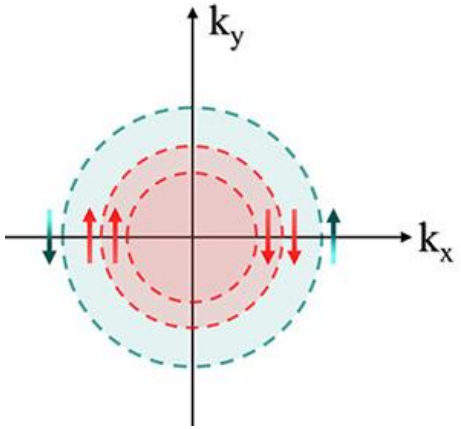



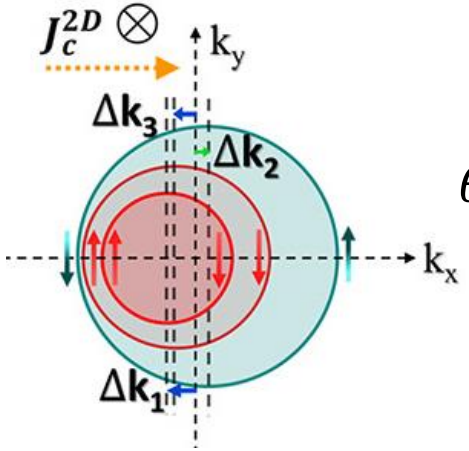




$\theta_{SOC} \propto \Delta k$

Topological Insulator
+
Insert



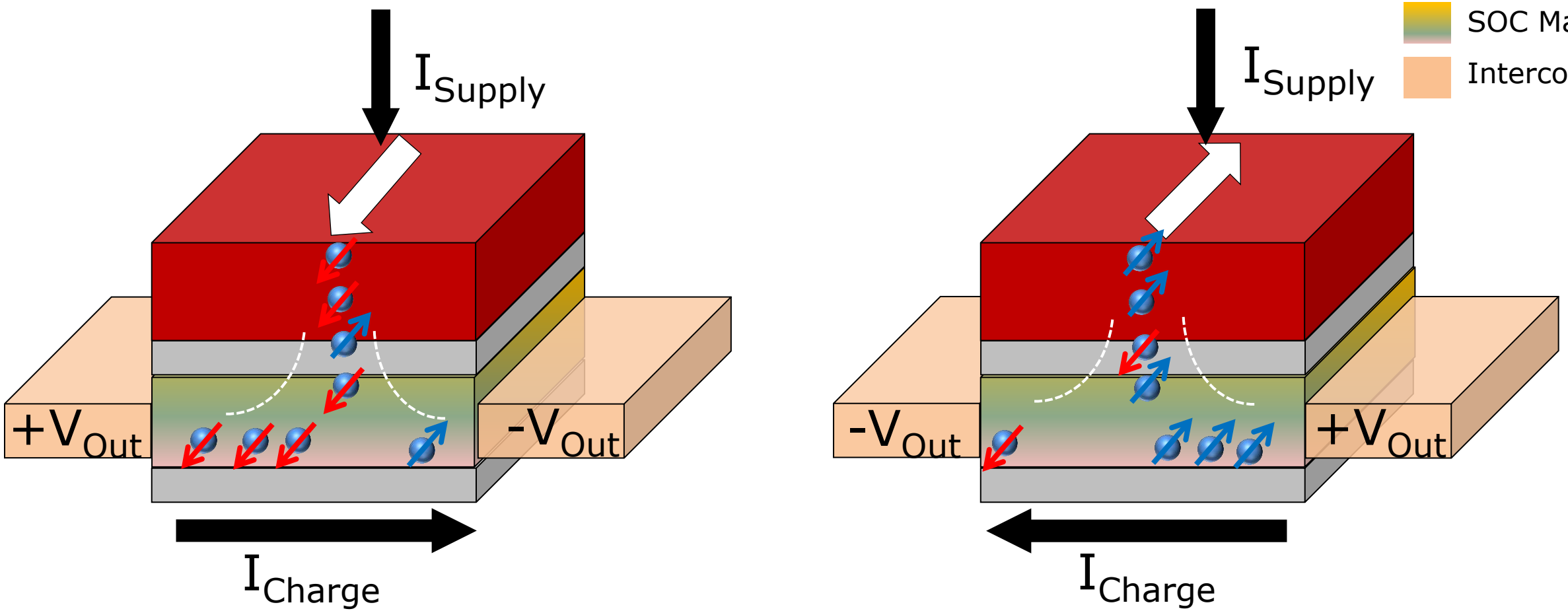




$\theta_{SOC} \propto \Delta k_1 - \Delta k_2 + \Delta k_3$

**Depending on the sign of spin orbit coupling of the new surface states they can enhance or reduce $\theta_{SOC}$. Doping in TI needs careful study but is promising.**

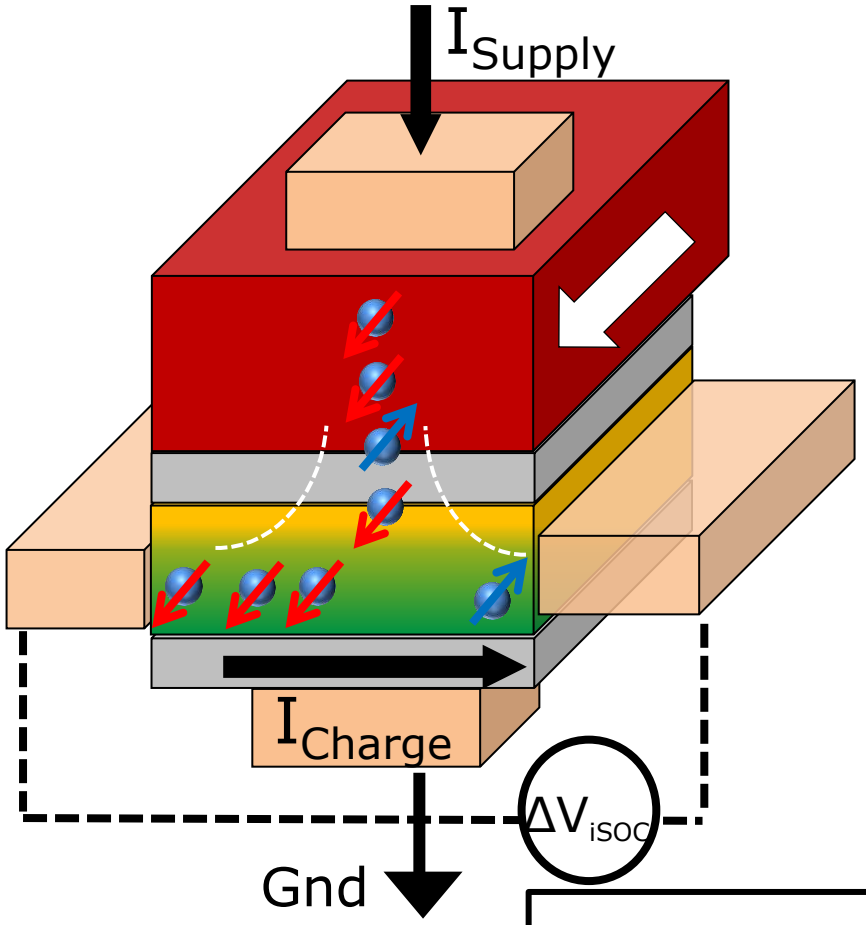
# Spin Orbit Module – Reads Magnetization

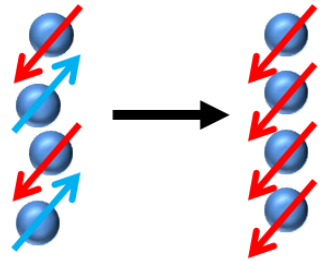



**Direction of the magnet controls the direction of the charge output**

**Direction of current determines the sign of input voltage for next stage → Cascading**

# Spin Orbit Module – Material Functionality



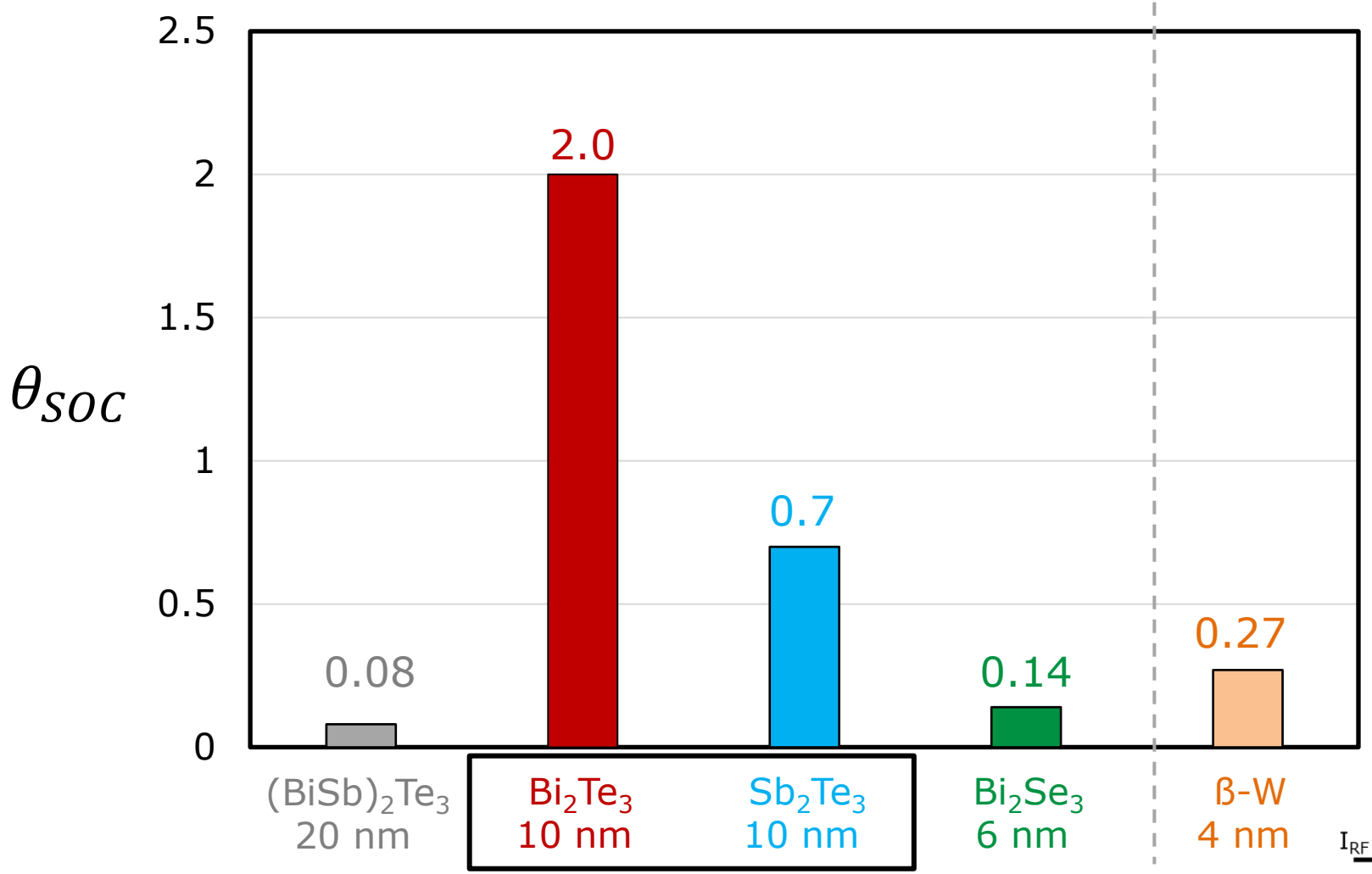
- Ferromagnet
  - → Polarization : $P_{FM}$
- Spin orbit coupling material
  - → Resistivity: $\rho_{SOC}$
  - → Spin to Charge efficiency: $\theta_{SOC}$
  - → Spin diffusion length: $\lambda_{sd}$
- Geometric Factors

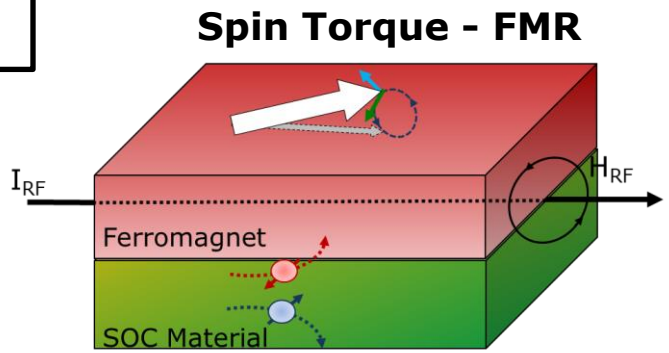
$$\frac{\Delta V_{isoc}}{I_{Supply}} = P_{FM}\,\rho_{SOC}\,\theta_{SOC}\,\lambda_{sd}\,\frac{1}{t_{SOC}w_{SOC}}\tanh\left(\frac{t_{SOC}}{2\lambda_{sd}}\right)$$

**Topological Insulators have high $\rho_{SOC}$ and large $\theta_{SOC}$**

$I_{Supply} = 10\mu A$

# $\theta_{SOC}$ Measurement Results for Topological Insulators

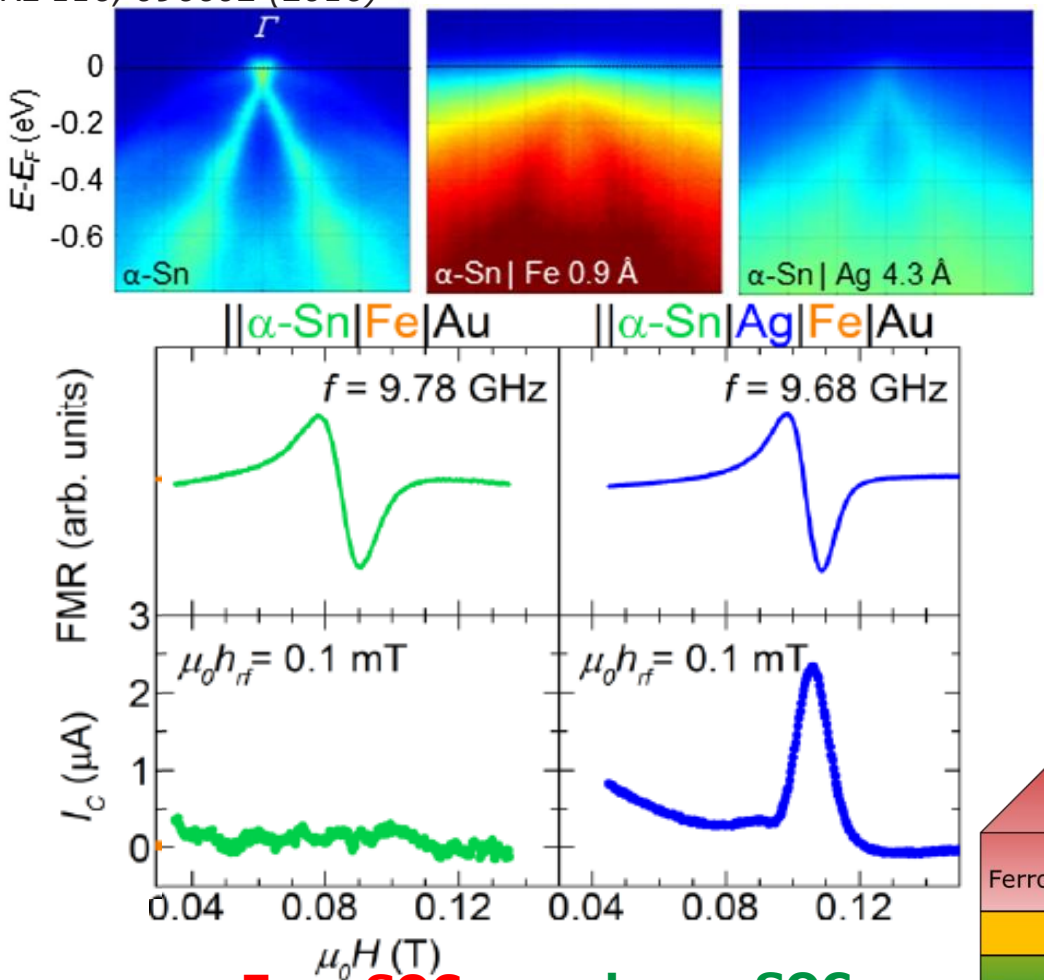


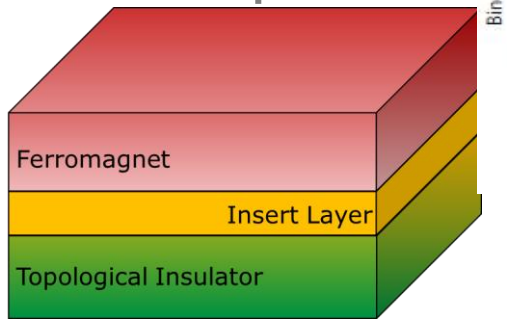

**Topological Insulators have large $\theta_{SOC}$**

# Optimizing Spin to Charge conversion in TI

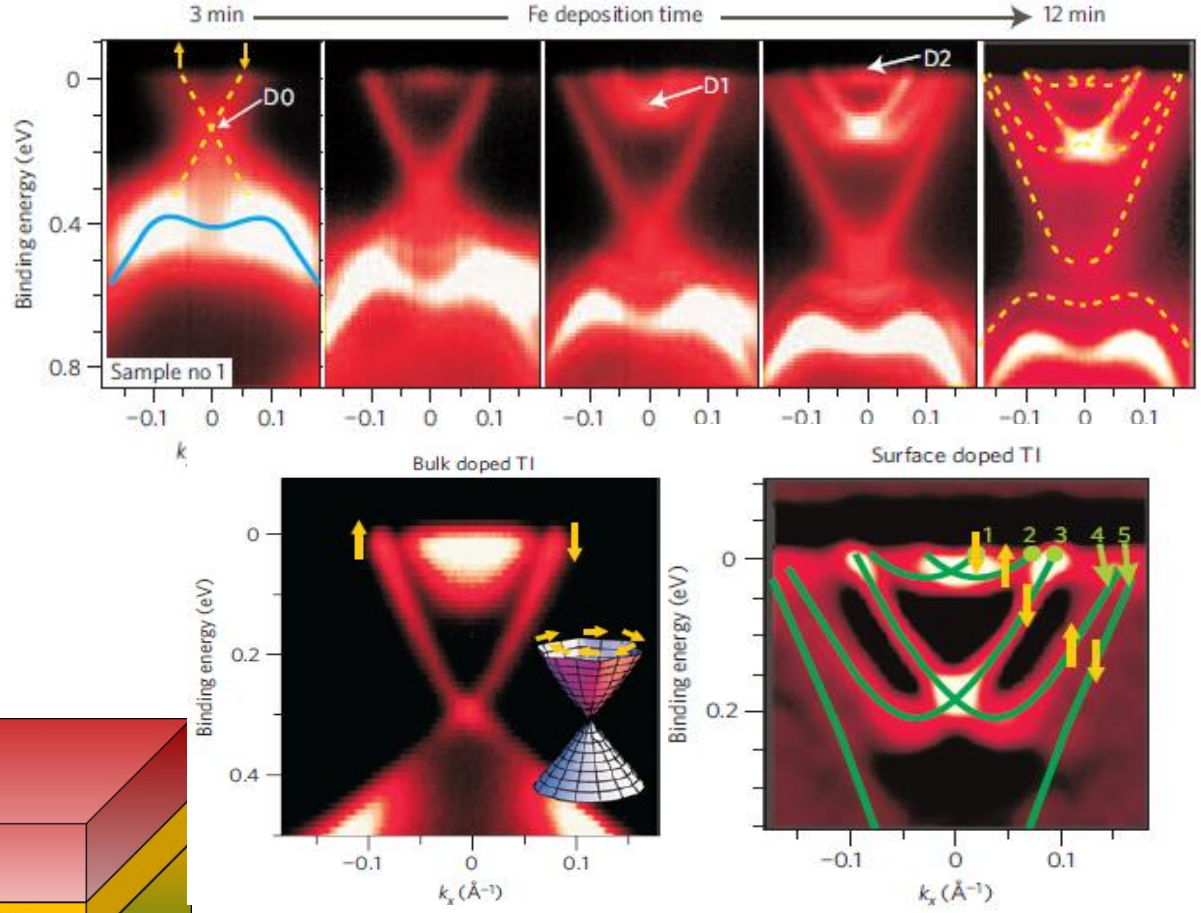
*PRL 116, 096602 (2016)*




**Zero SOC** **Large SOC**



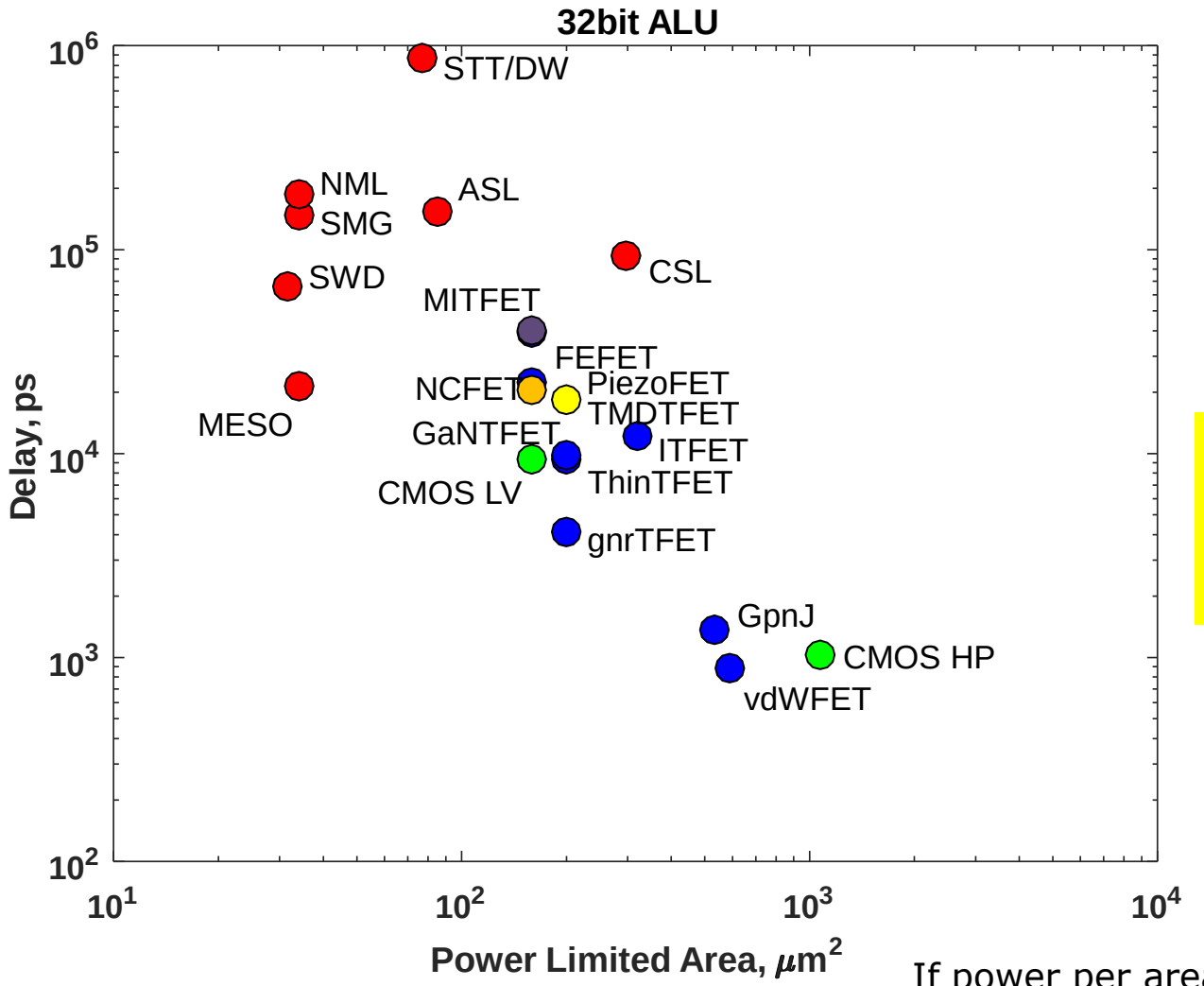

*Nature Physics 7, 32–37(2011)*

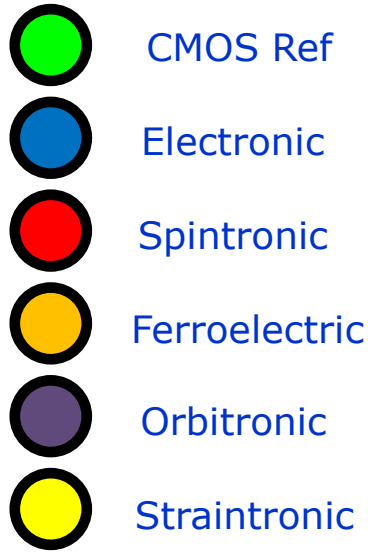



**1 Surface State → 5 Surface States**

**Doping TI with insert layer can protect the surface states and also enhance $\theta_{SOC}$.**

# Delay vs. Area

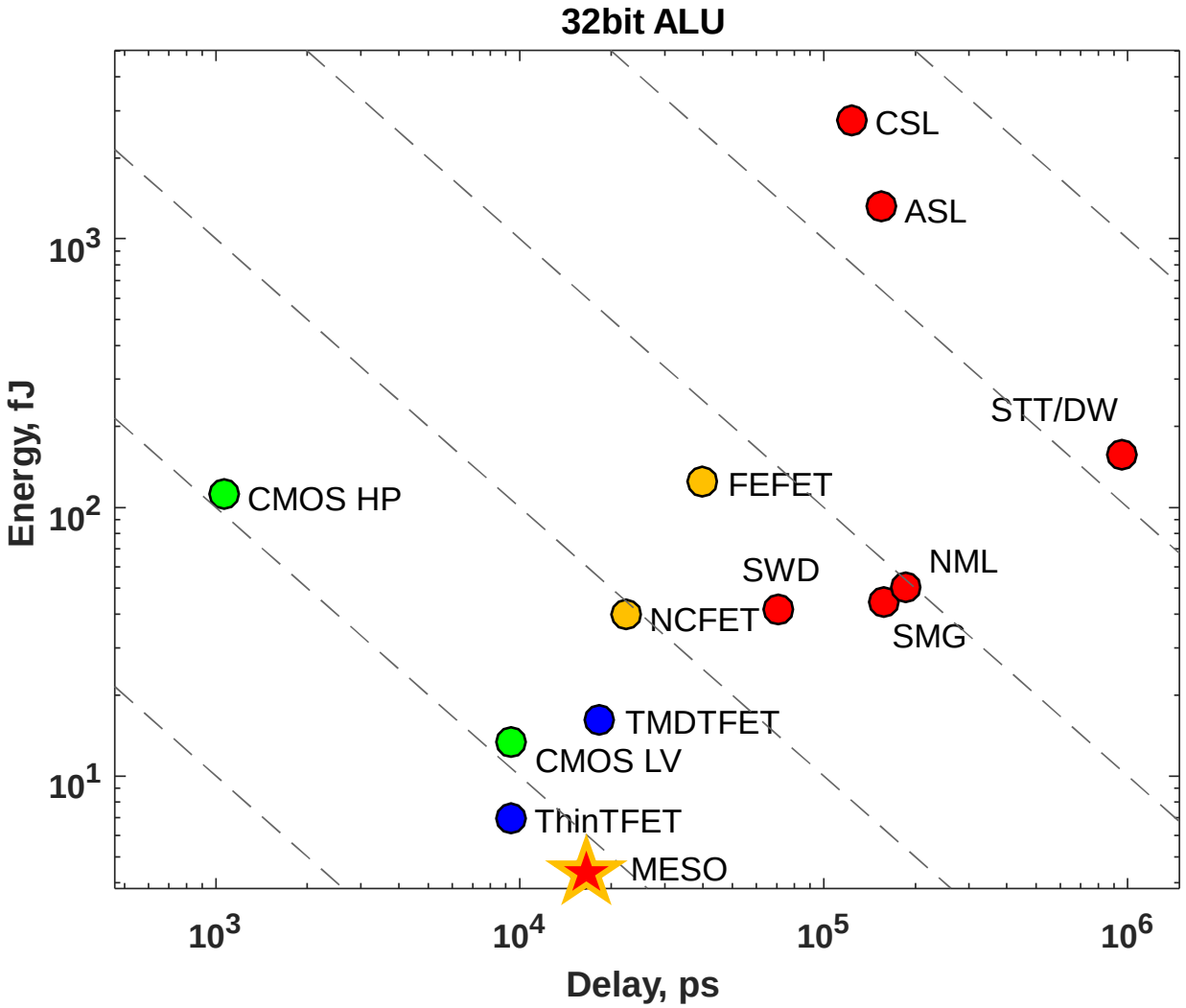



**Spintronics is slower than electronics, but more compact**

If power per area exceed the cap (10W/cm$^2$), effective area is rescaled to be larger

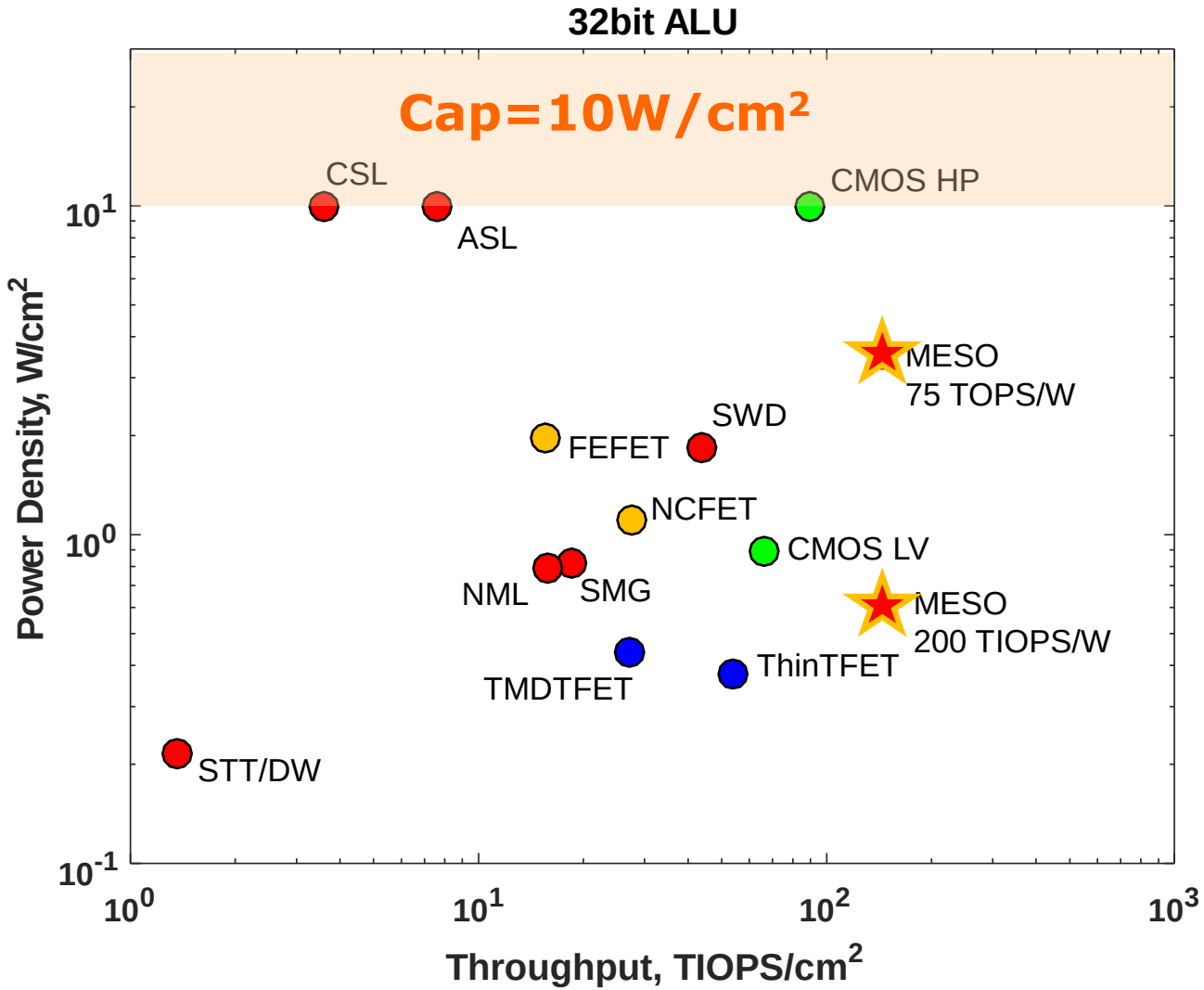
# Exchange Bias and Exchange Coupling




- MESO is >10x lower energy than high-performance CMOS
- At the expense of slower speed
- Went through this trade off around 1990: transition from bipolar to CMOS transistors

D. E. Nikonov and I. A. Young, IEEE J. Explor. Comput. Devices and Circuits 1, 3-11 (2015).

# Exchange Bias and Exchange Coupling




- CMOS is limited by dissipated power density
- Exhibited as the capability to remove heat from the chip, but mostly power available to the data center
- MESO is not limited by power, can achieve higher computing throughput (!)

S. Manipatruni et al., Nature 565 (7737), 35-42 (2019).

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